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Narayanasamy

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(54) **CIRCUIT AND SYSTEM FOR THE REDUCTION OF VOLTAGE OVERTHOOT IN POWER SWITCHES**

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(51) **Int. Cl.**

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H03K 17/06 (2006.01)
H03K 17/08 (2006.01)
H03K 17/28 (2006.01)
H03K 17/60 (2006.01)

(52) **U.S. Cl.**

CPC **H03K 17/08** (2013.01); **H02M 1/08** (2013.01); **H03K 17/06** (2013.01); **H03K 17/28** (2013.01); **H03K 17/60** (2013.01)

(58) **Field of Classification Search**

CPC H02M 1/08; H03K 17/06; H03K 17/08; H03K 17/28; H03K 17/60
USPC 327/108, 109, 110, 111, 113, 114, 172, 327/176, 419, 478
See application file for complete search history.

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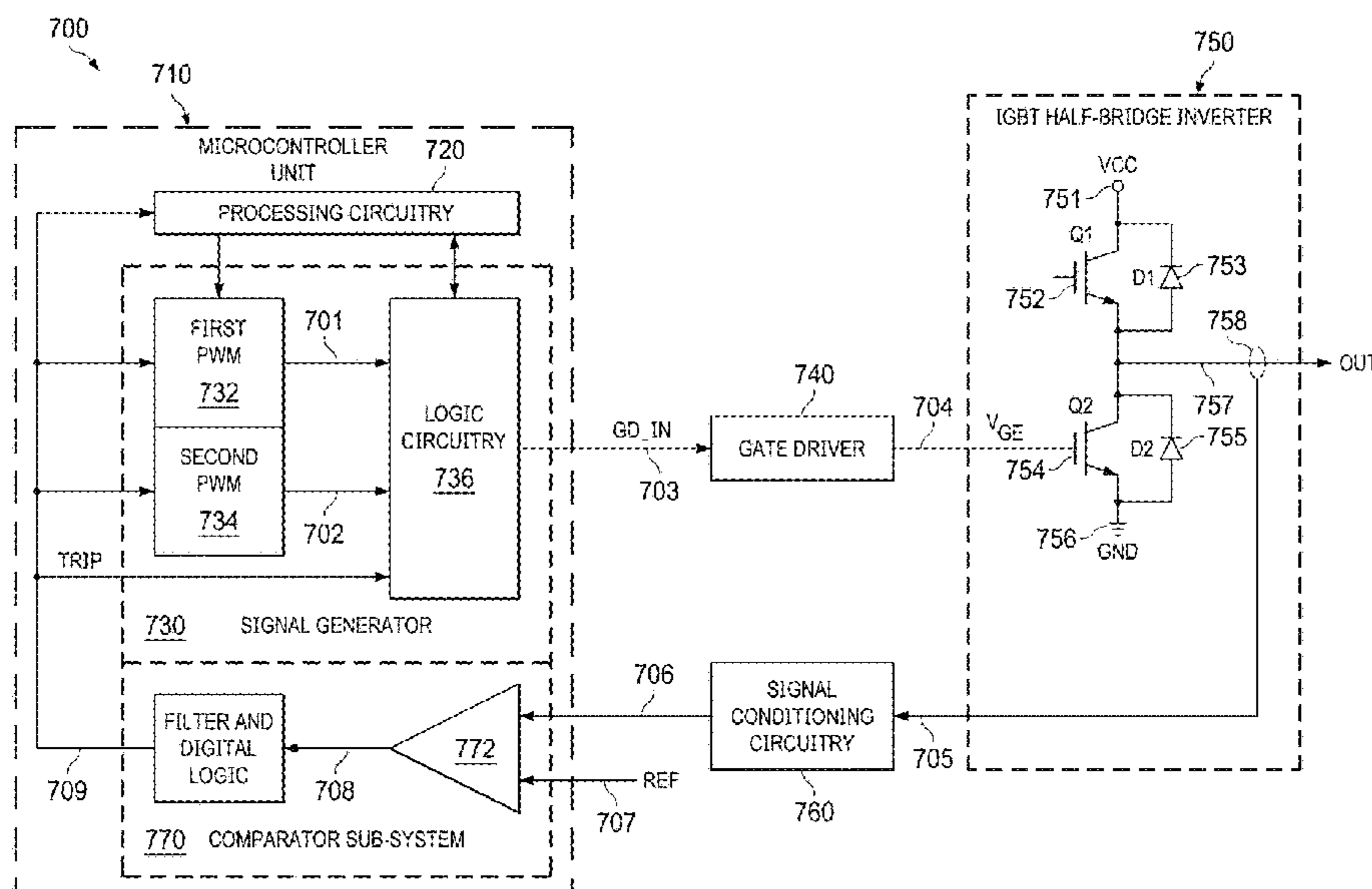
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(57) **ABSTRACT**

An electronic circuit for controlling a power switch having a gate input, includes a signal generator configured to generate a gate driver input signal. The gate driver input signal has a first voltage during a first period of time, a second voltage during a second period of time, and toggles between the first voltage and the second voltage during a third period of time. The electronic circuit also includes a gate driver configured to receive the gate driver input signal and to provide a gate driver output signal based on the gate driver input signal. The signal generator is configured to cause the gate driver input signal to toggle during the third period of time such that the gate driver output signal has a third voltage during the second period of time, and an intermediate voltage that is less than the third voltage during the third period of time.

20 Claims, 20 Drawing Sheets



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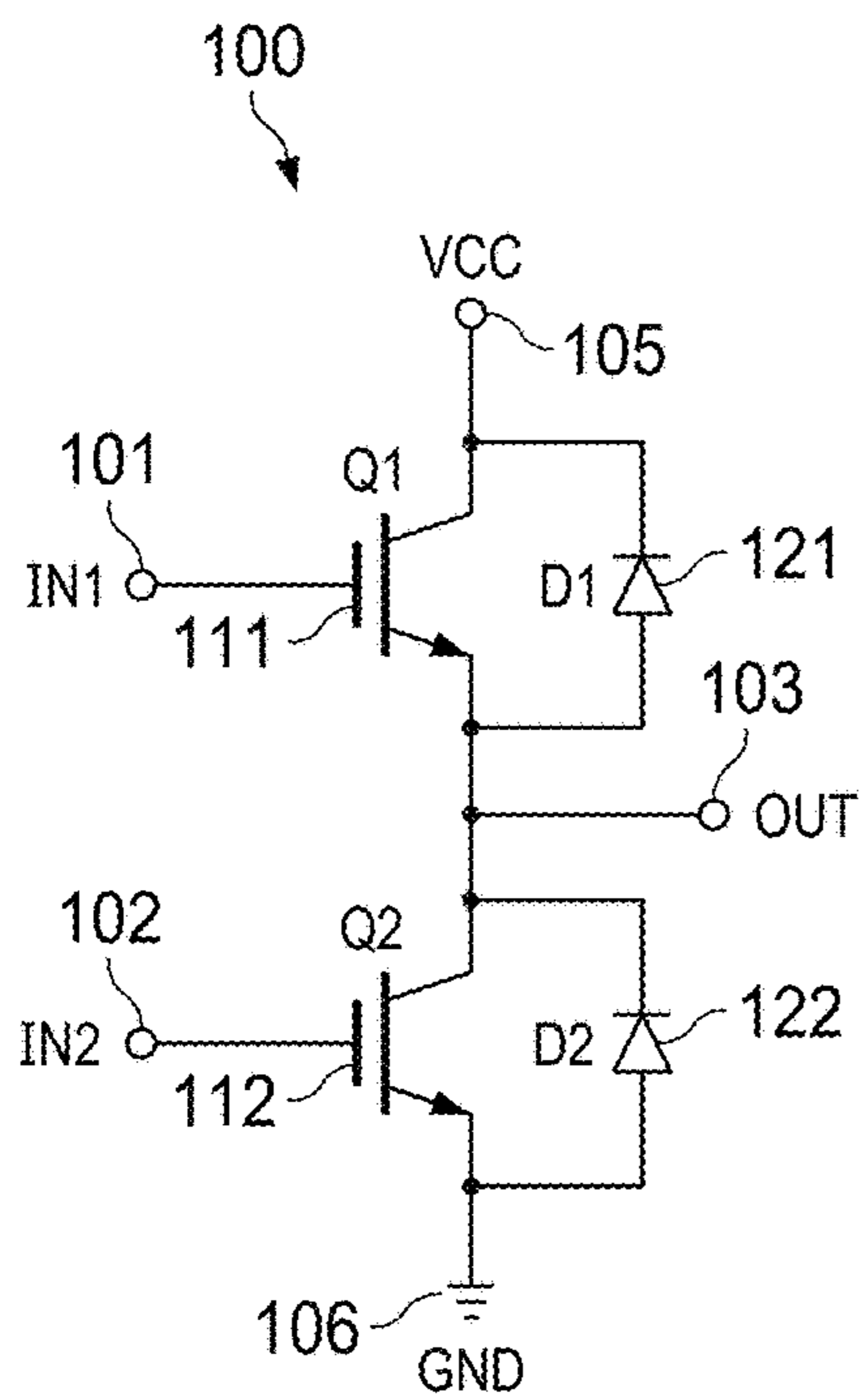


FIG. 1

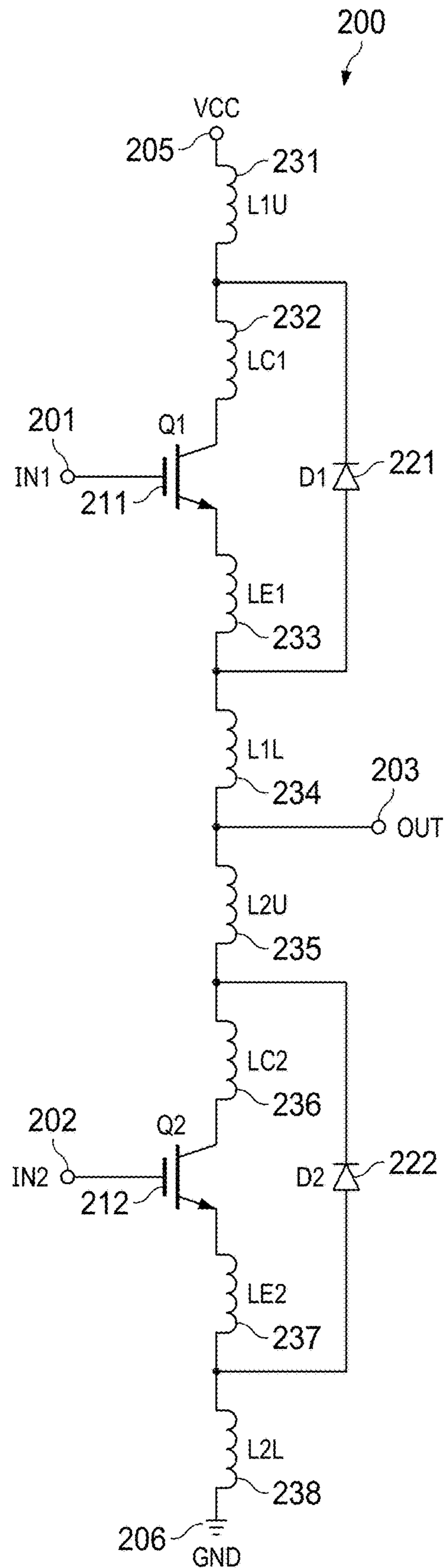


FIG. 2

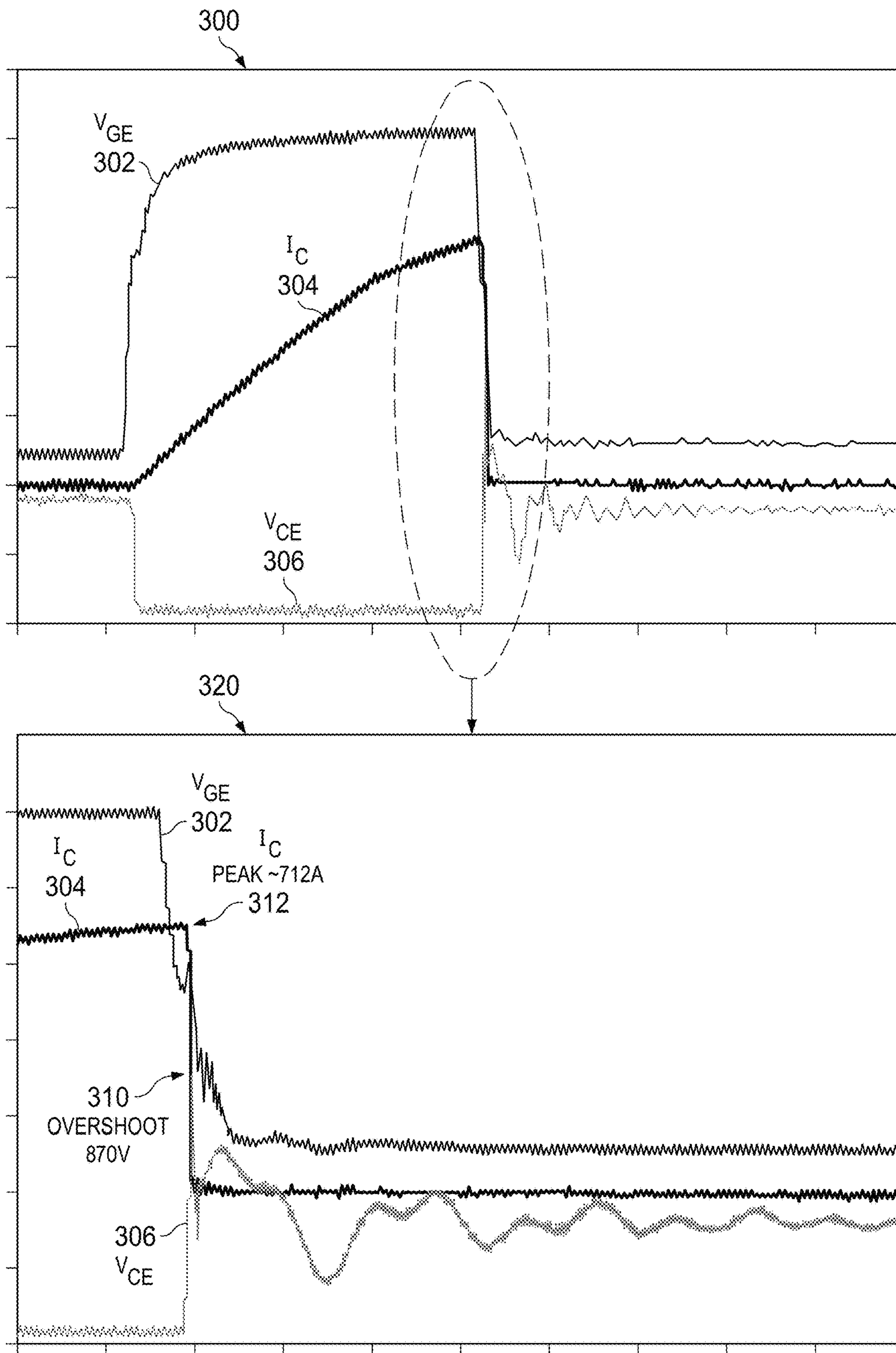


FIG. 3

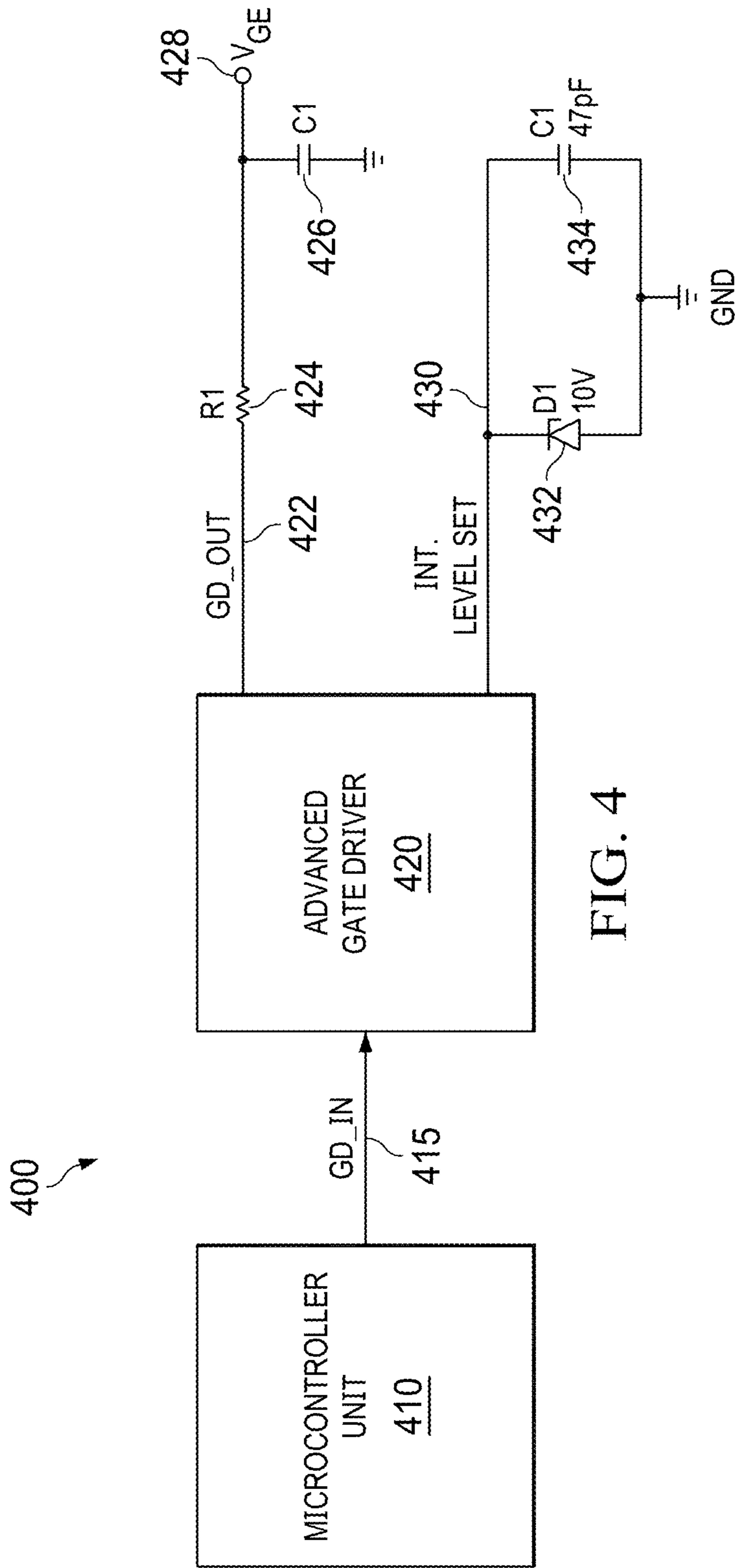


FIG. 4

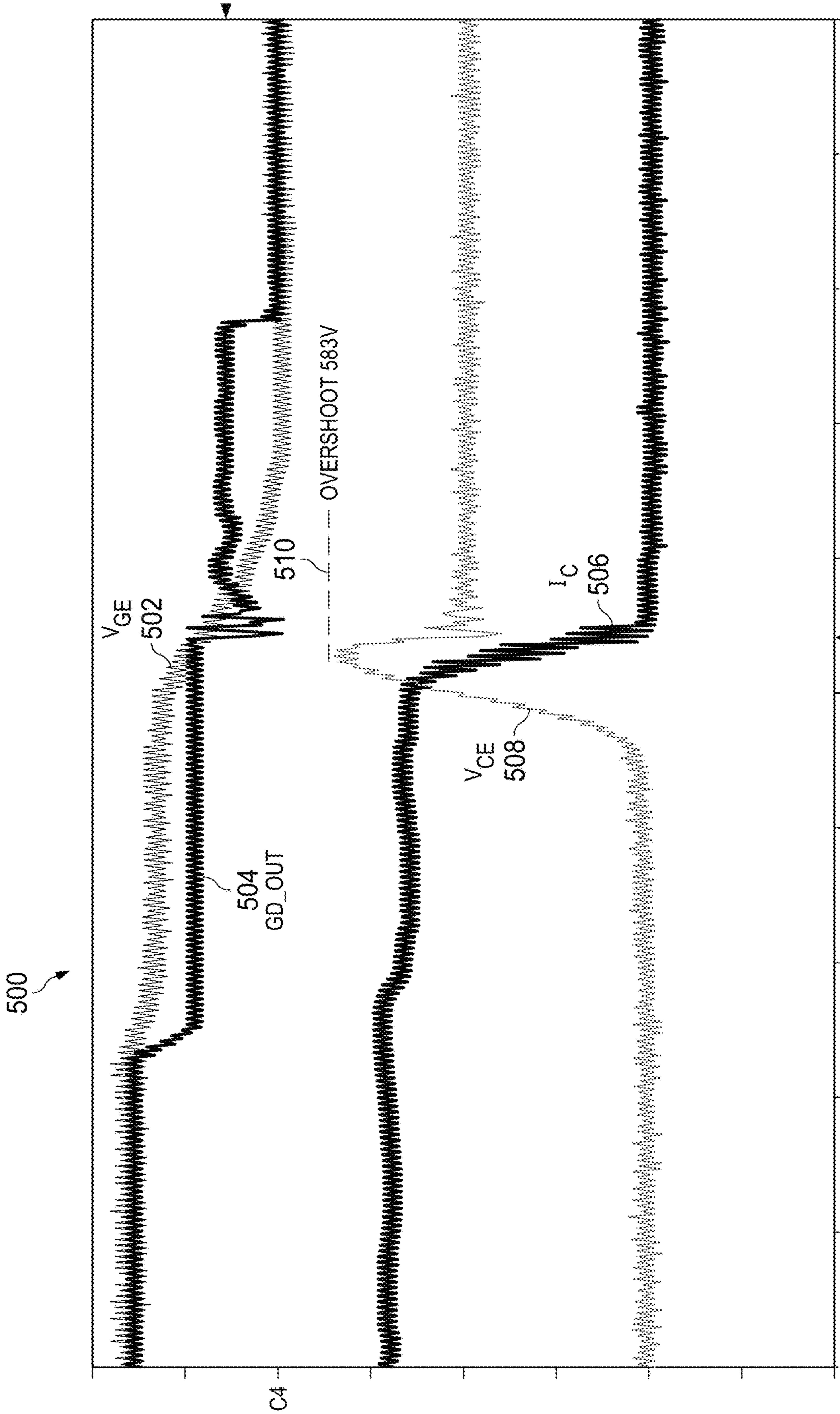


FIG. 5

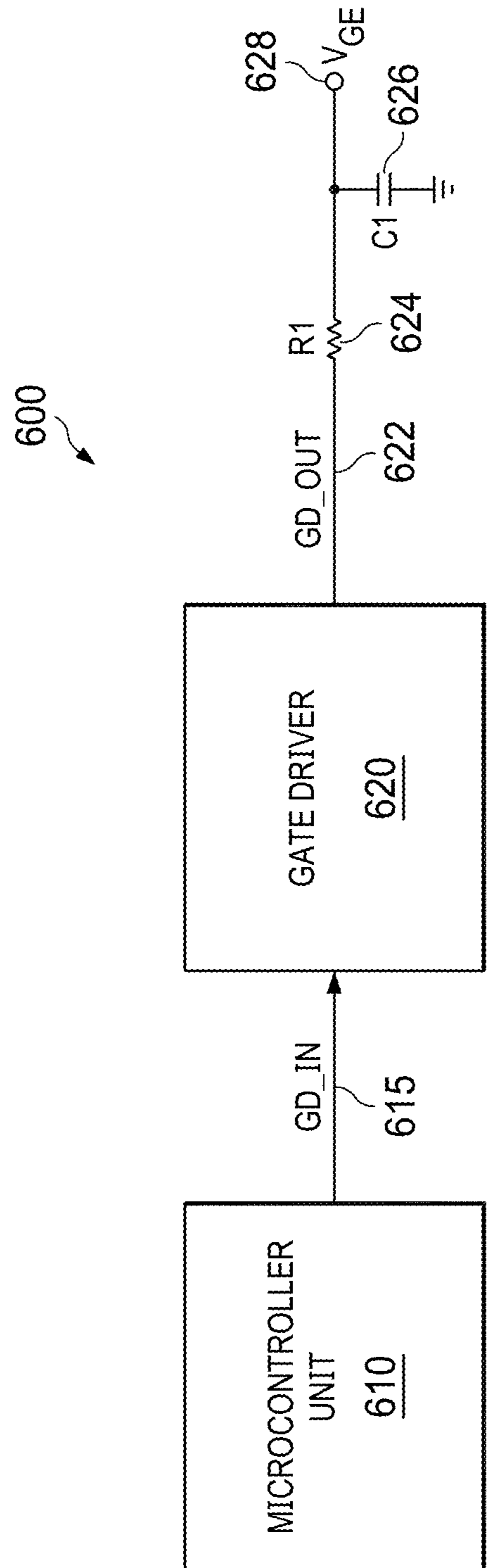


FIG. 6A

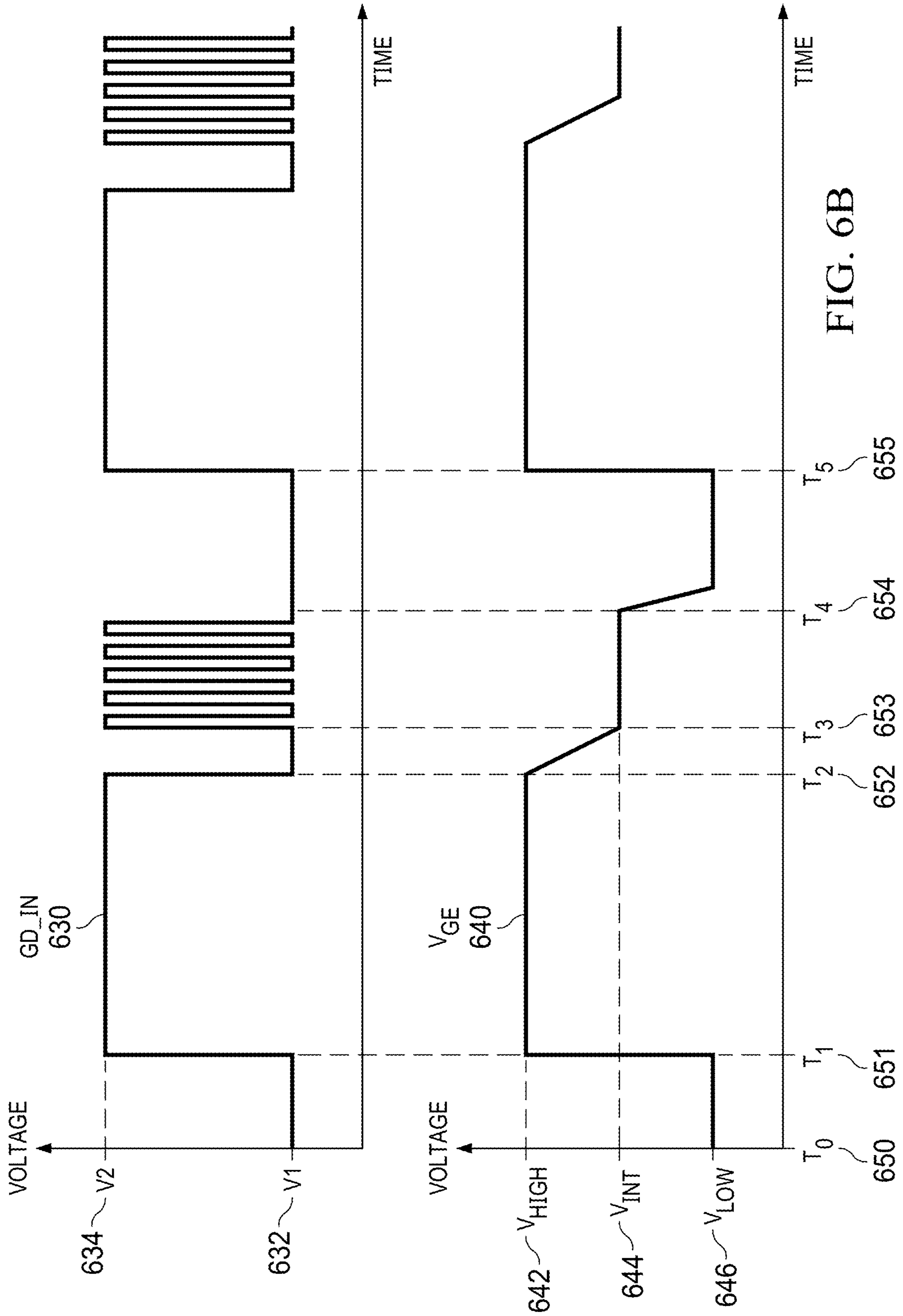


FIG. 6B

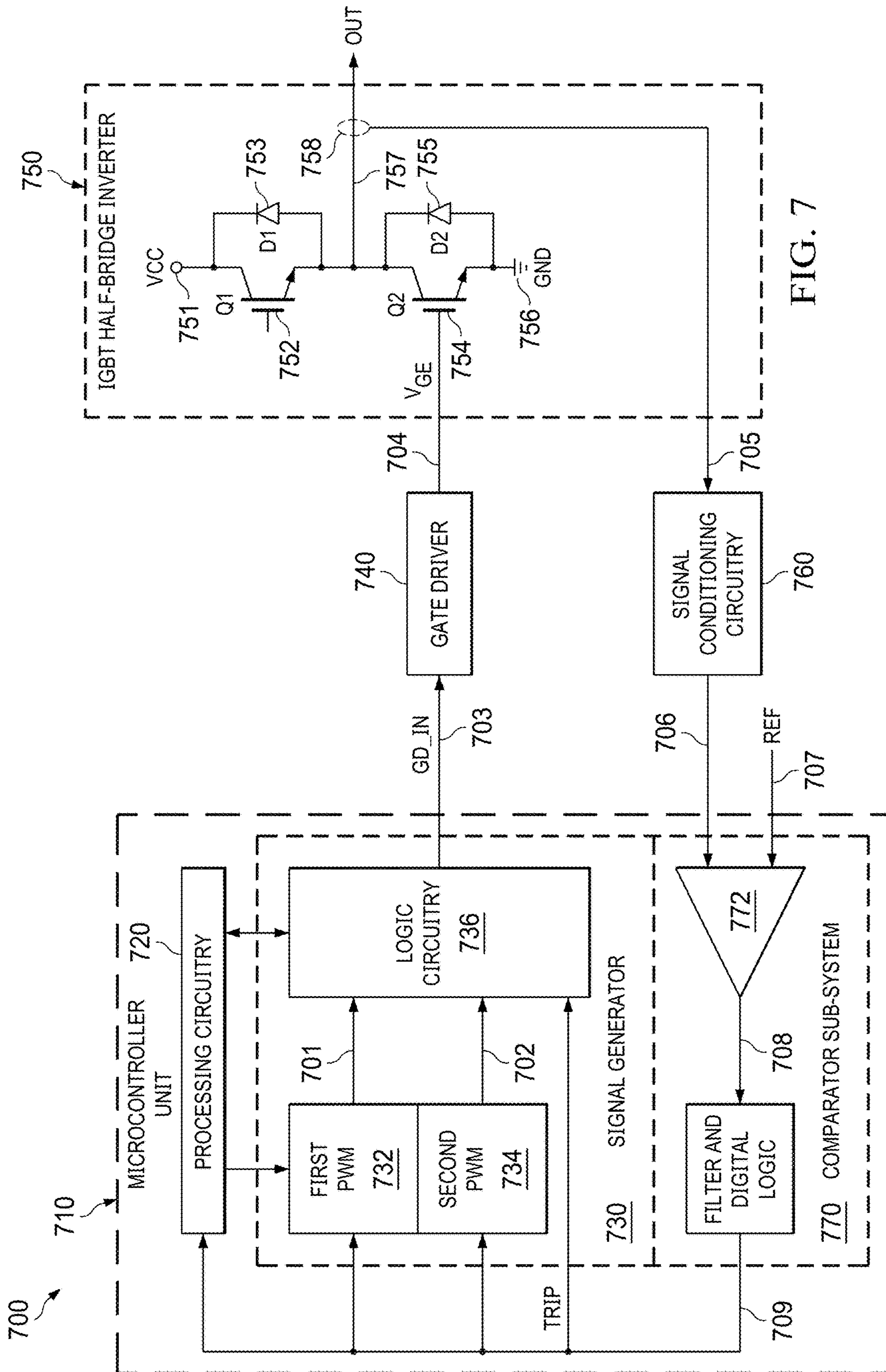


FIG. 7

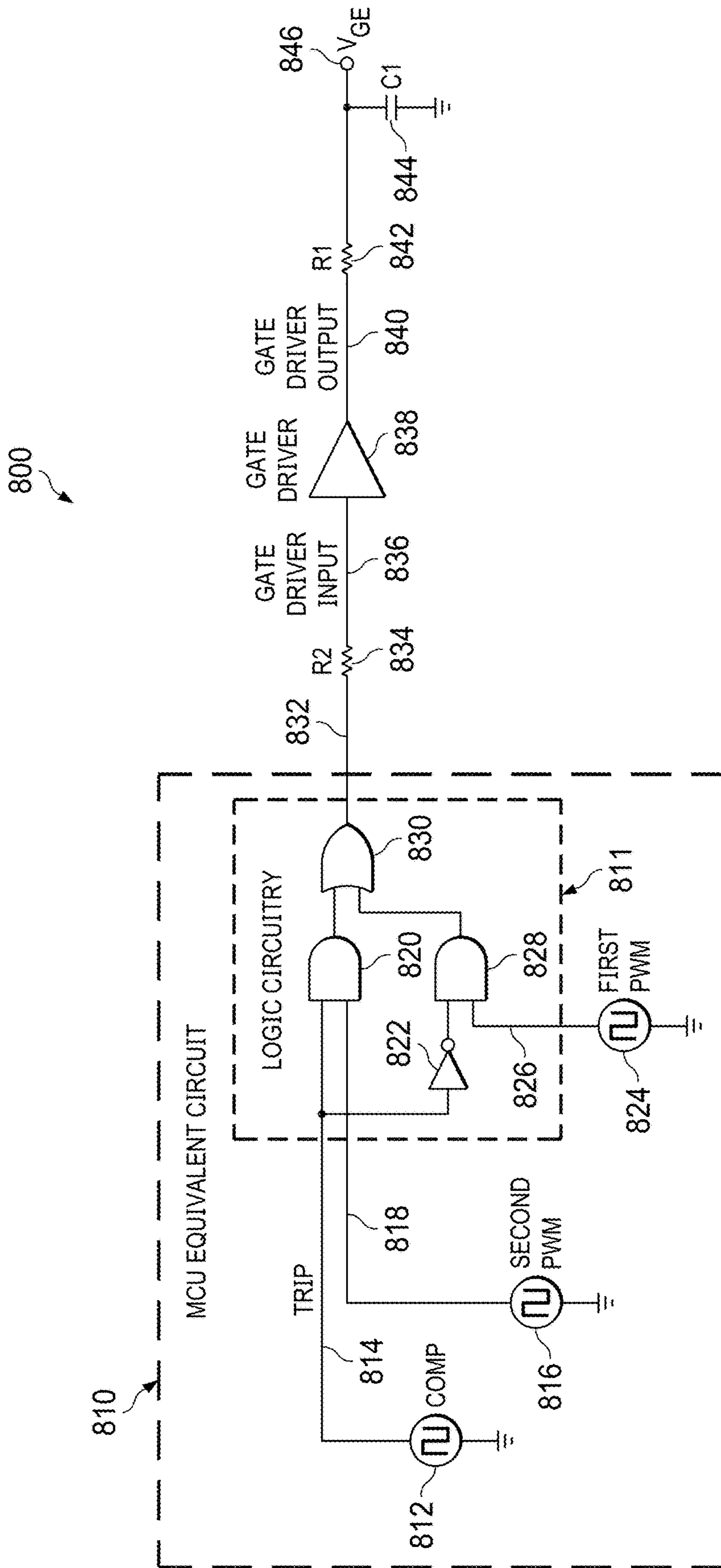


FIG. 8

FIG. 9

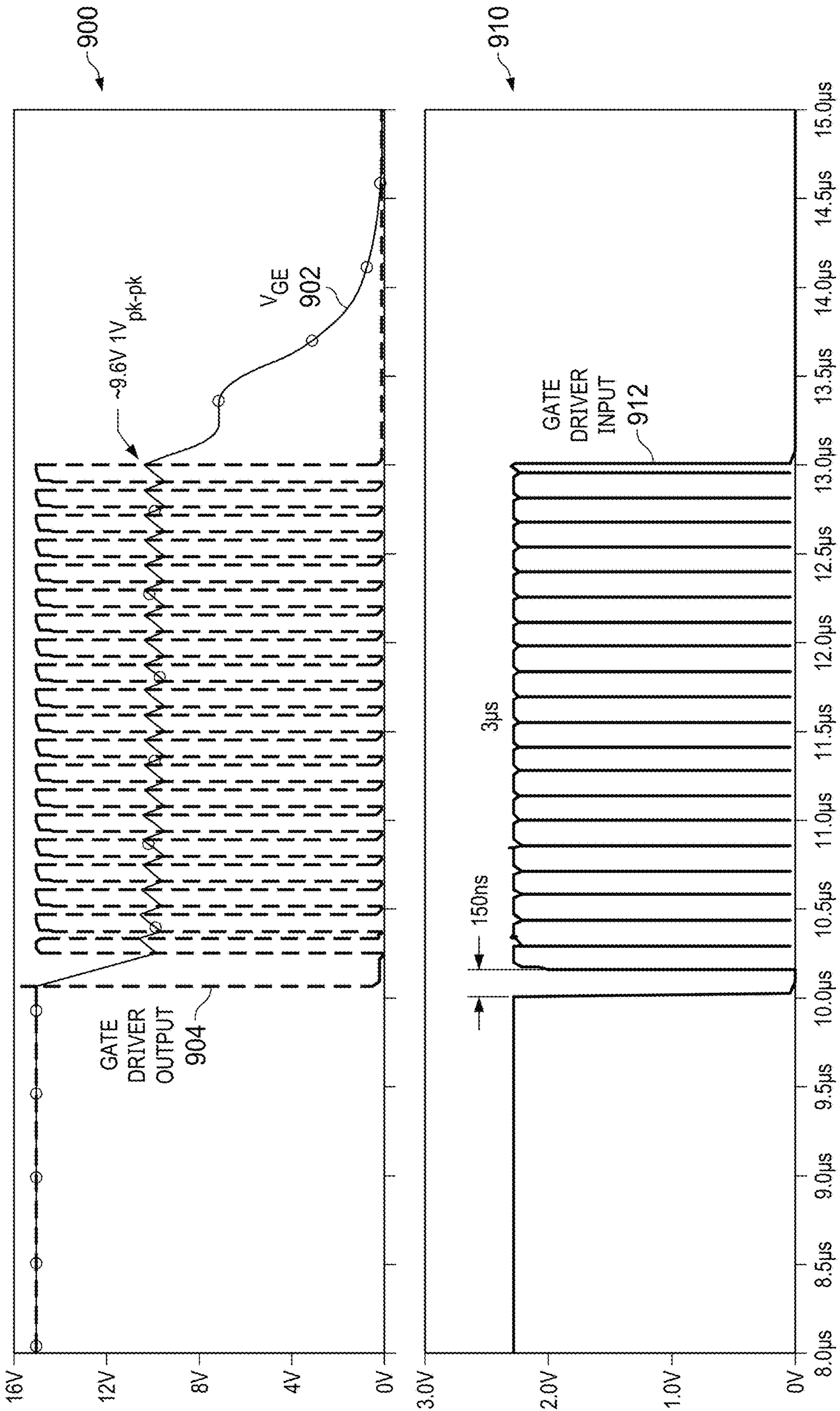
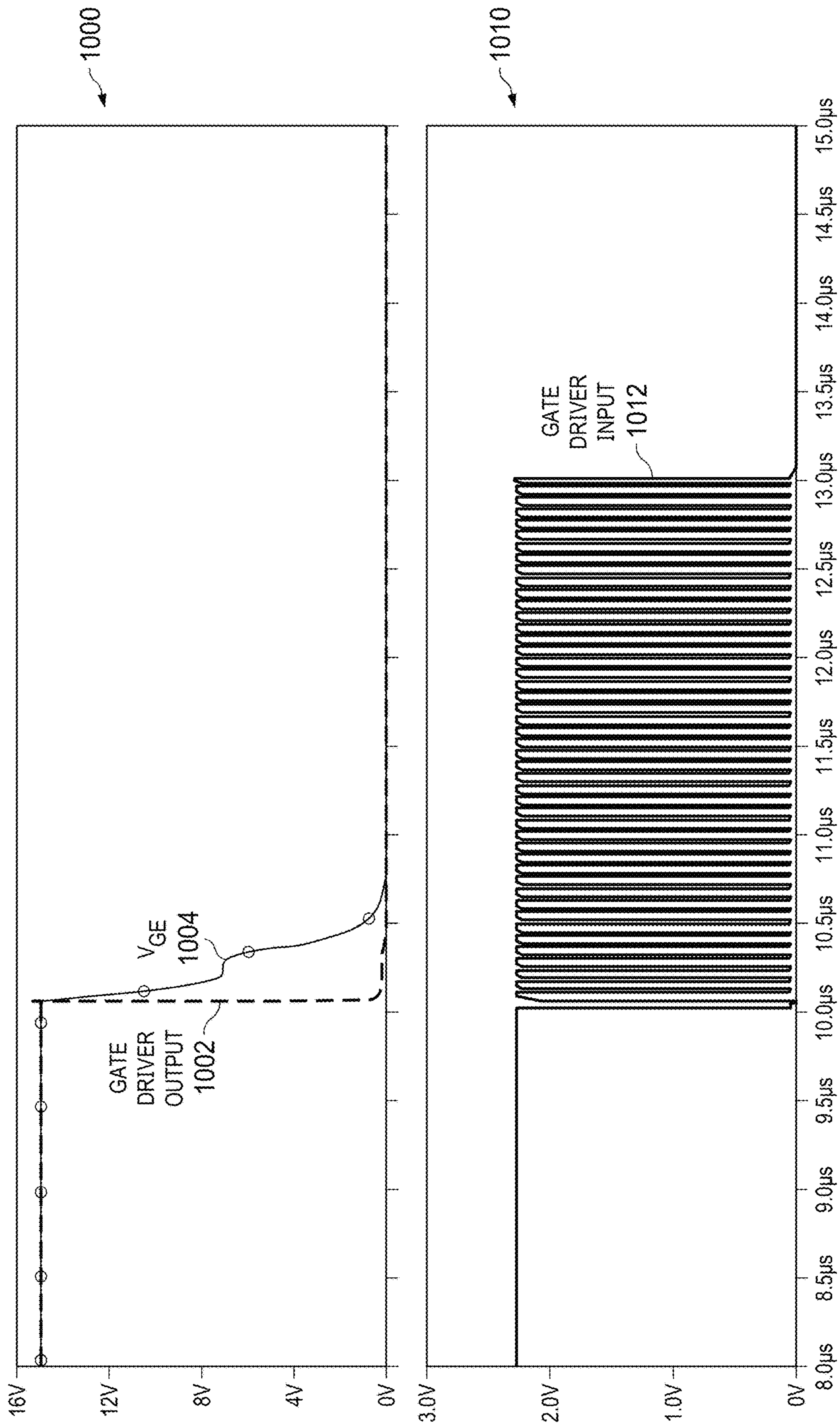
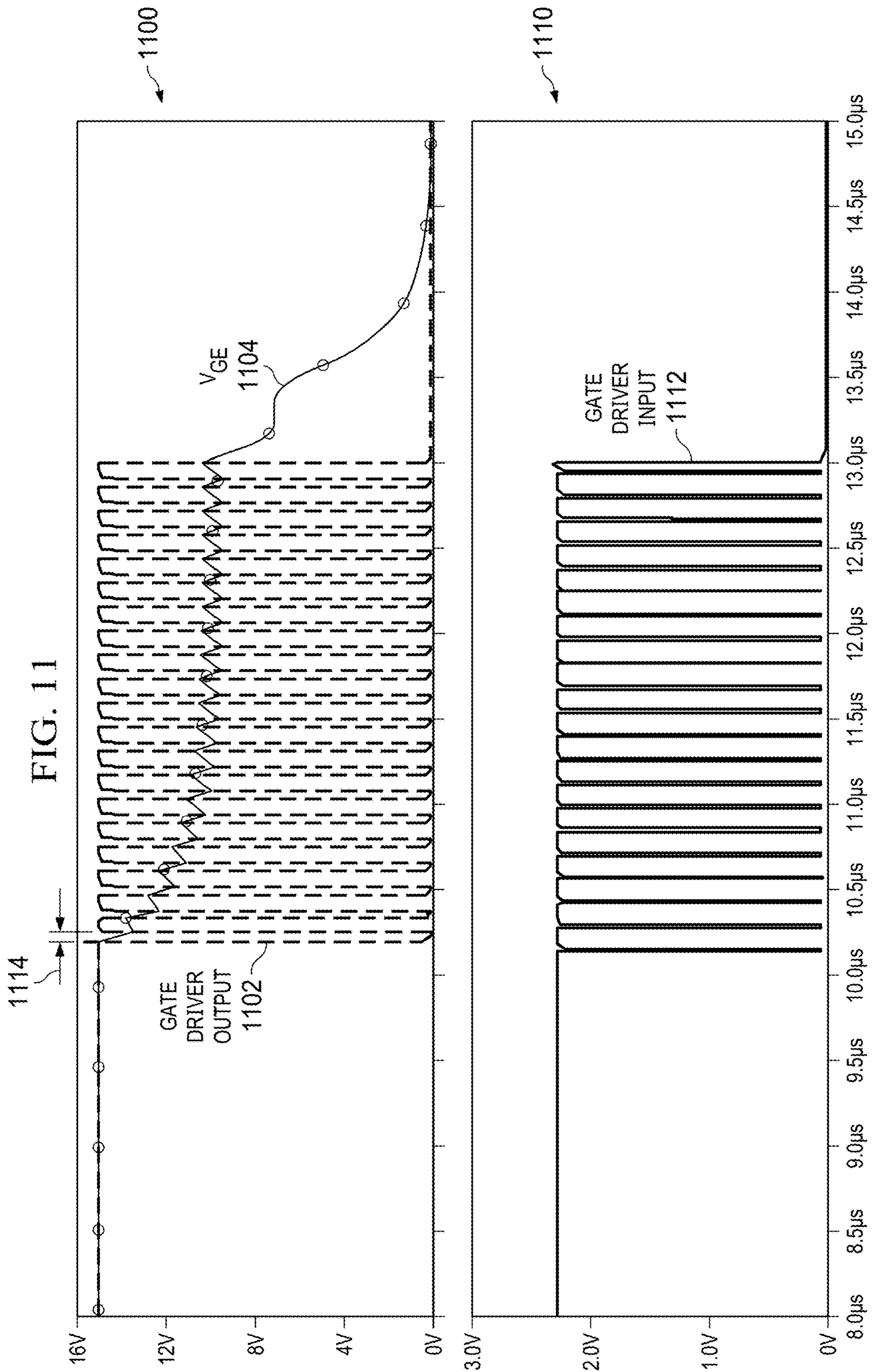


FIG. 10





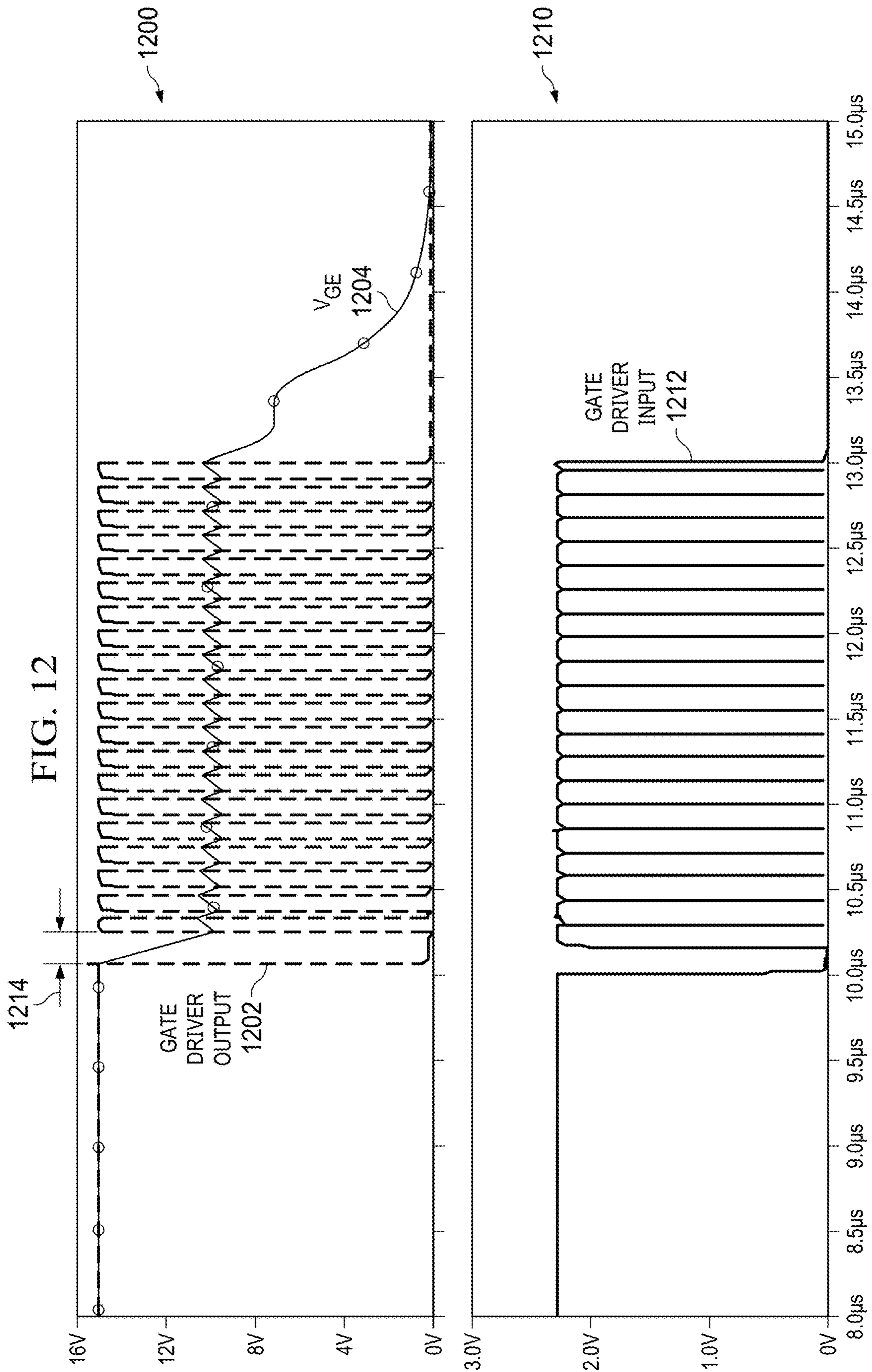


FIG. 13

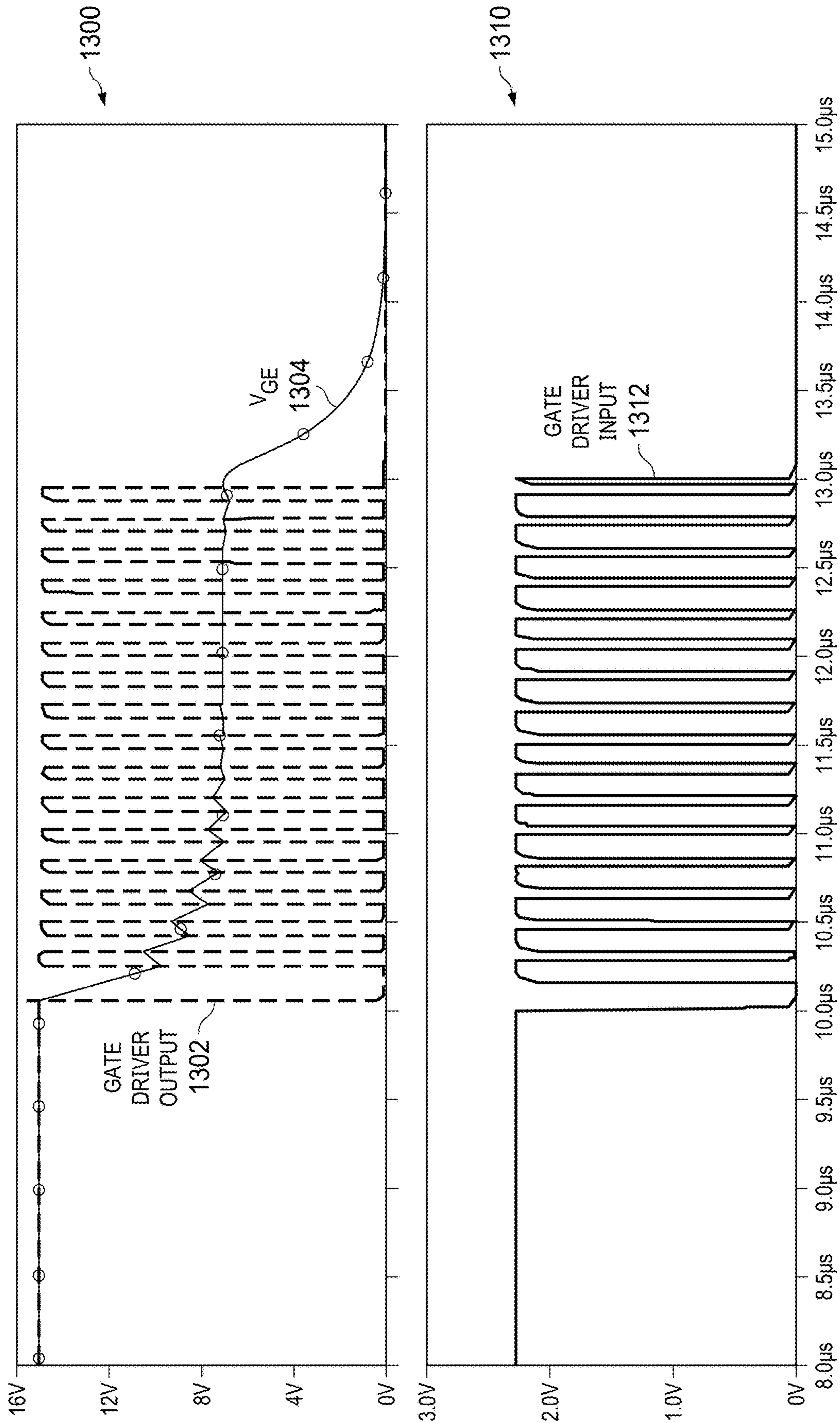


FIG. 14

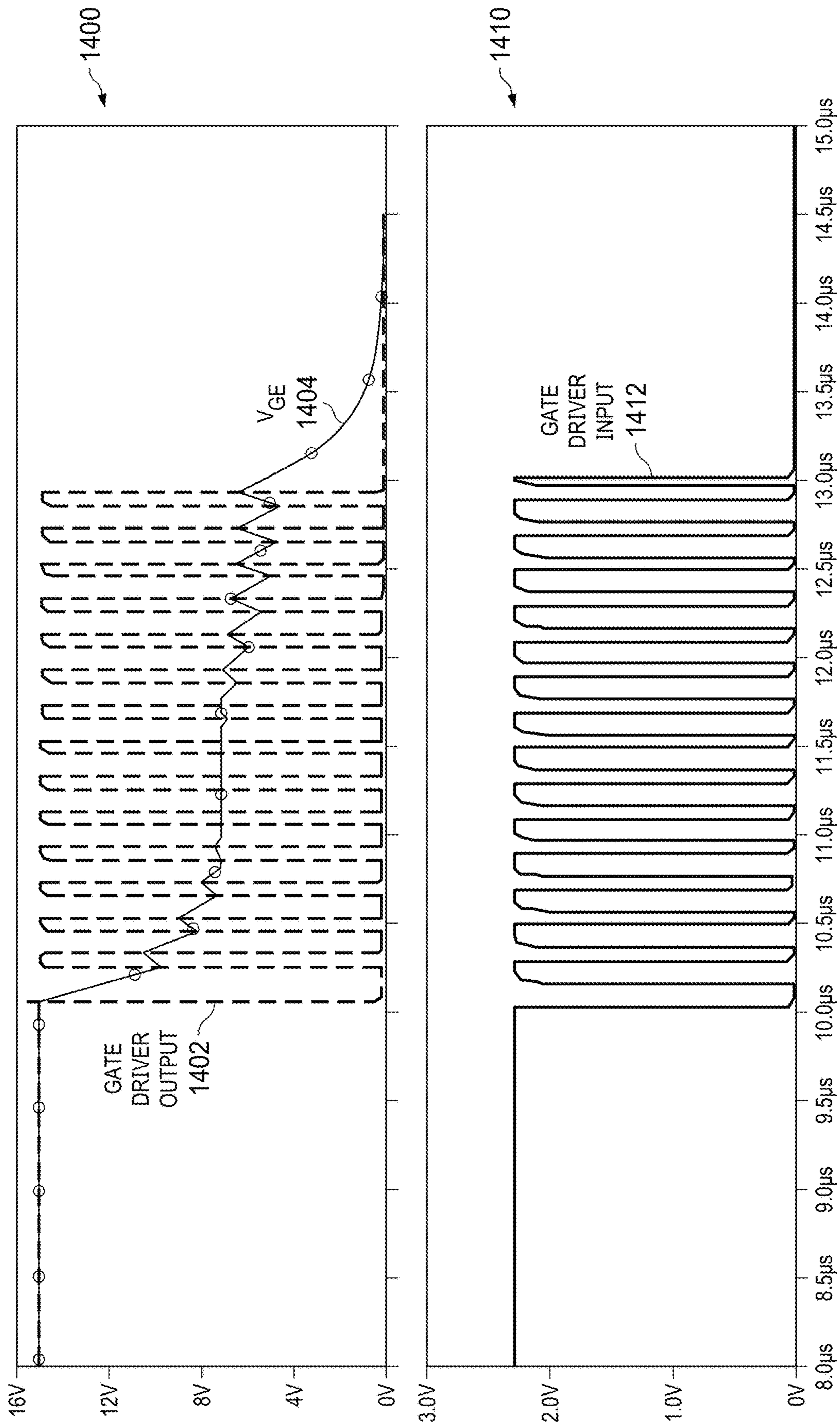


FIG. 15

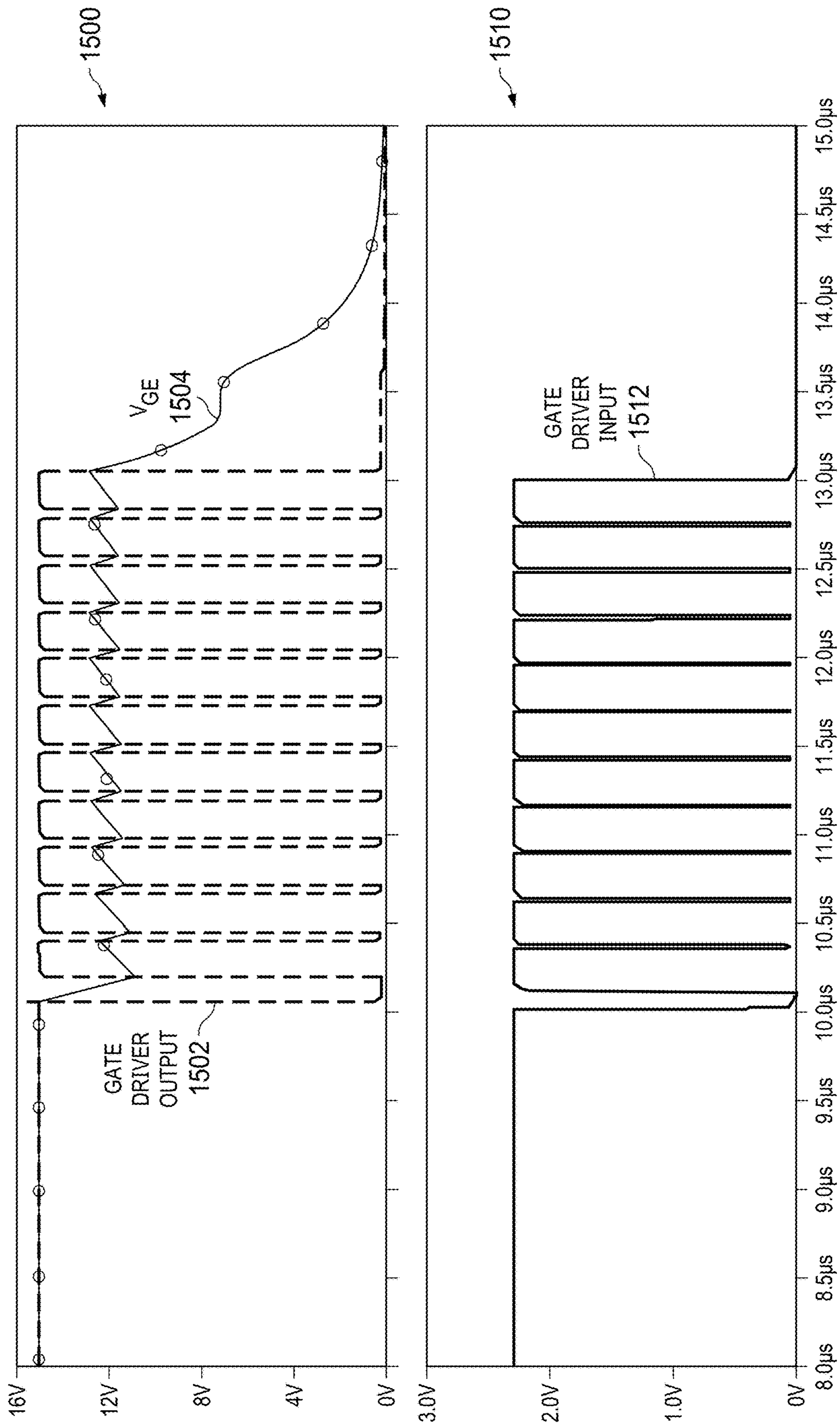


FIG. 16

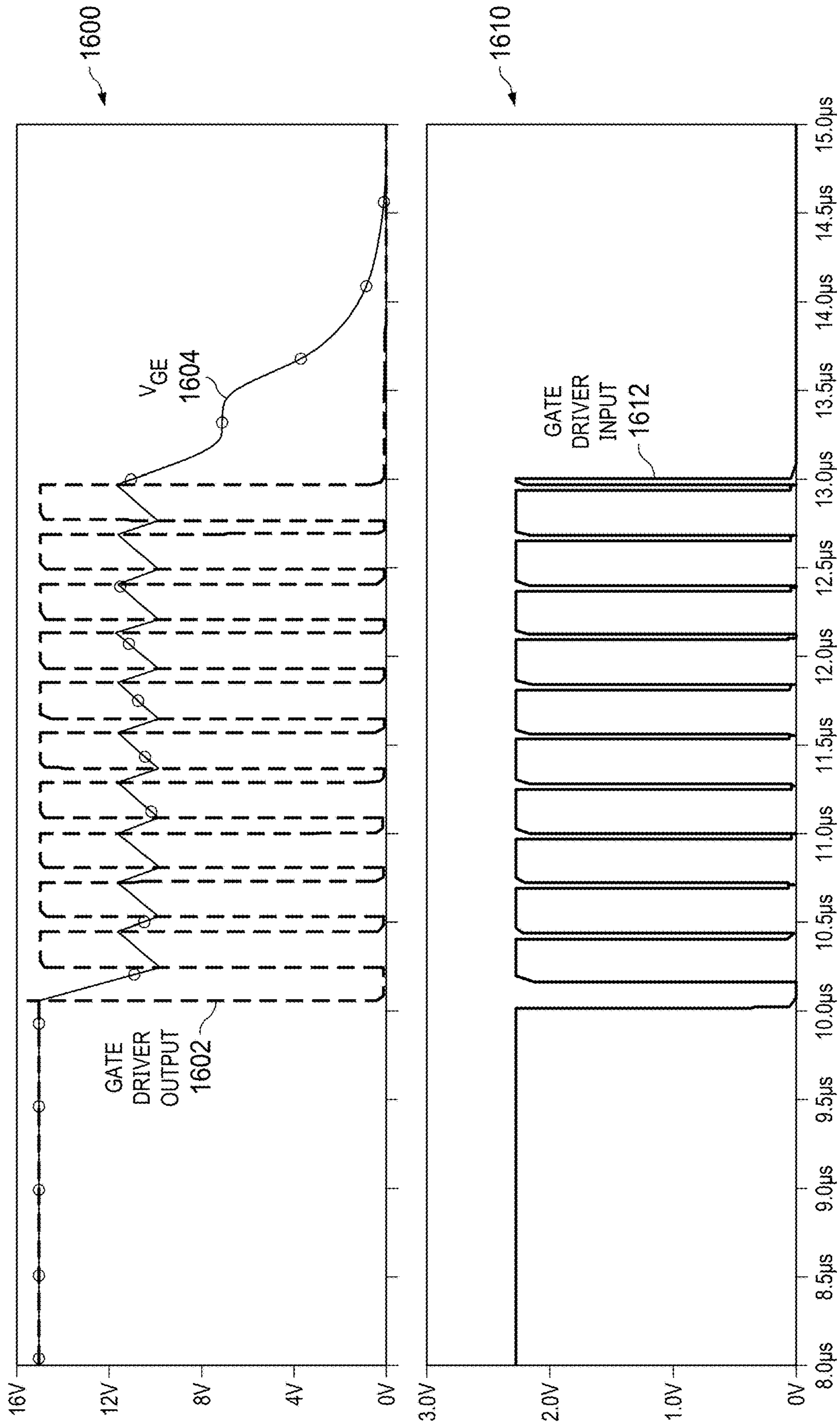


FIG. 17

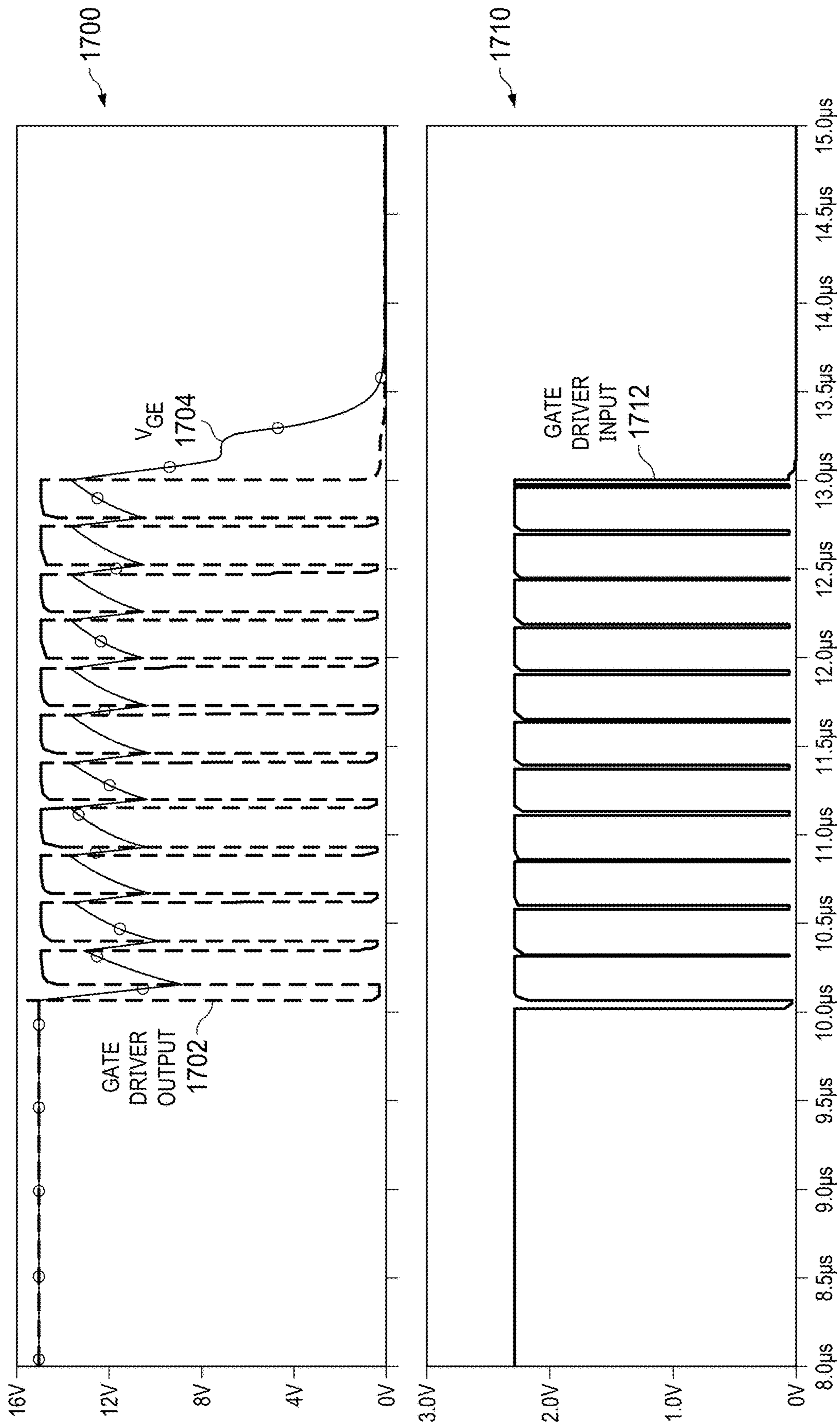
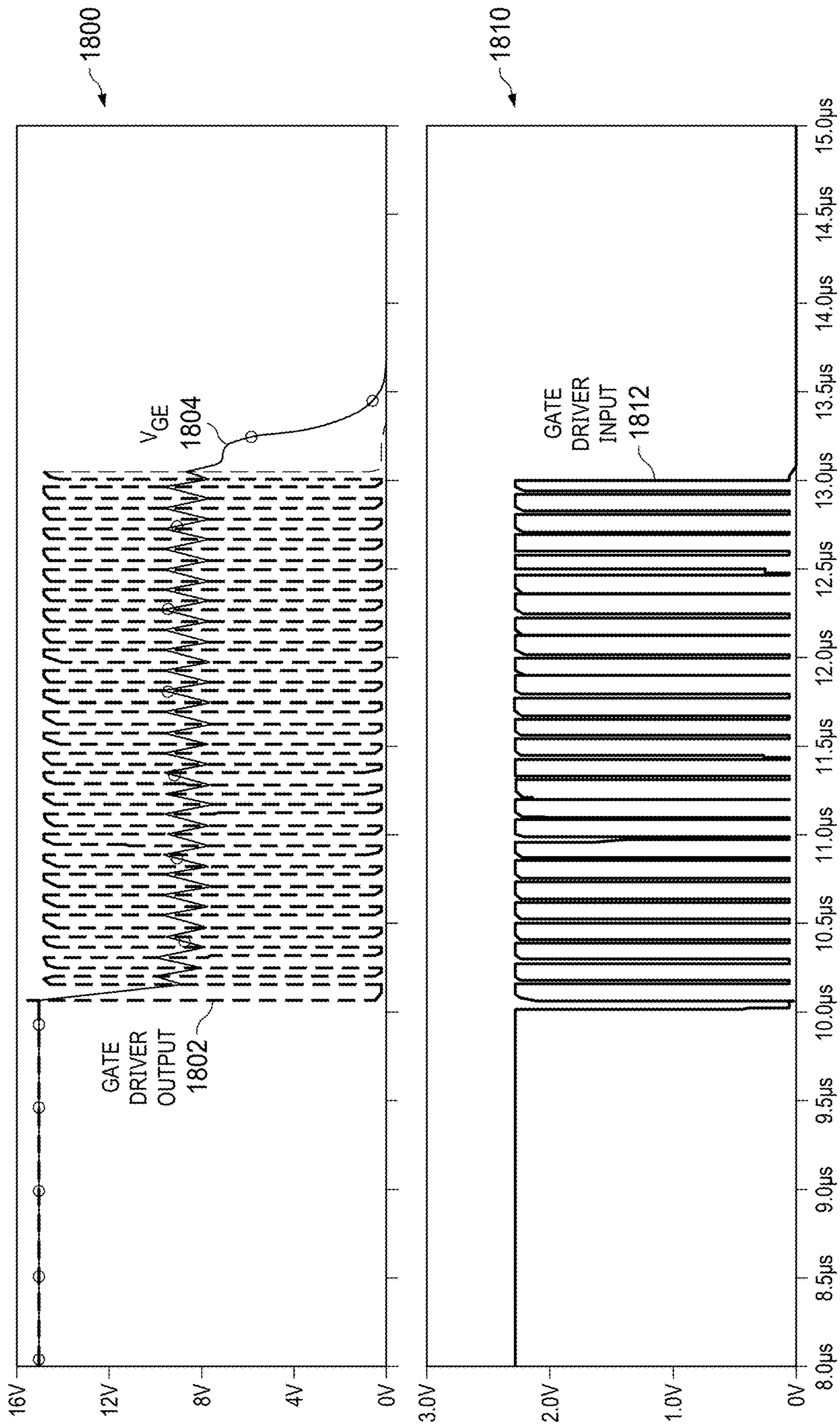


FIG. 18



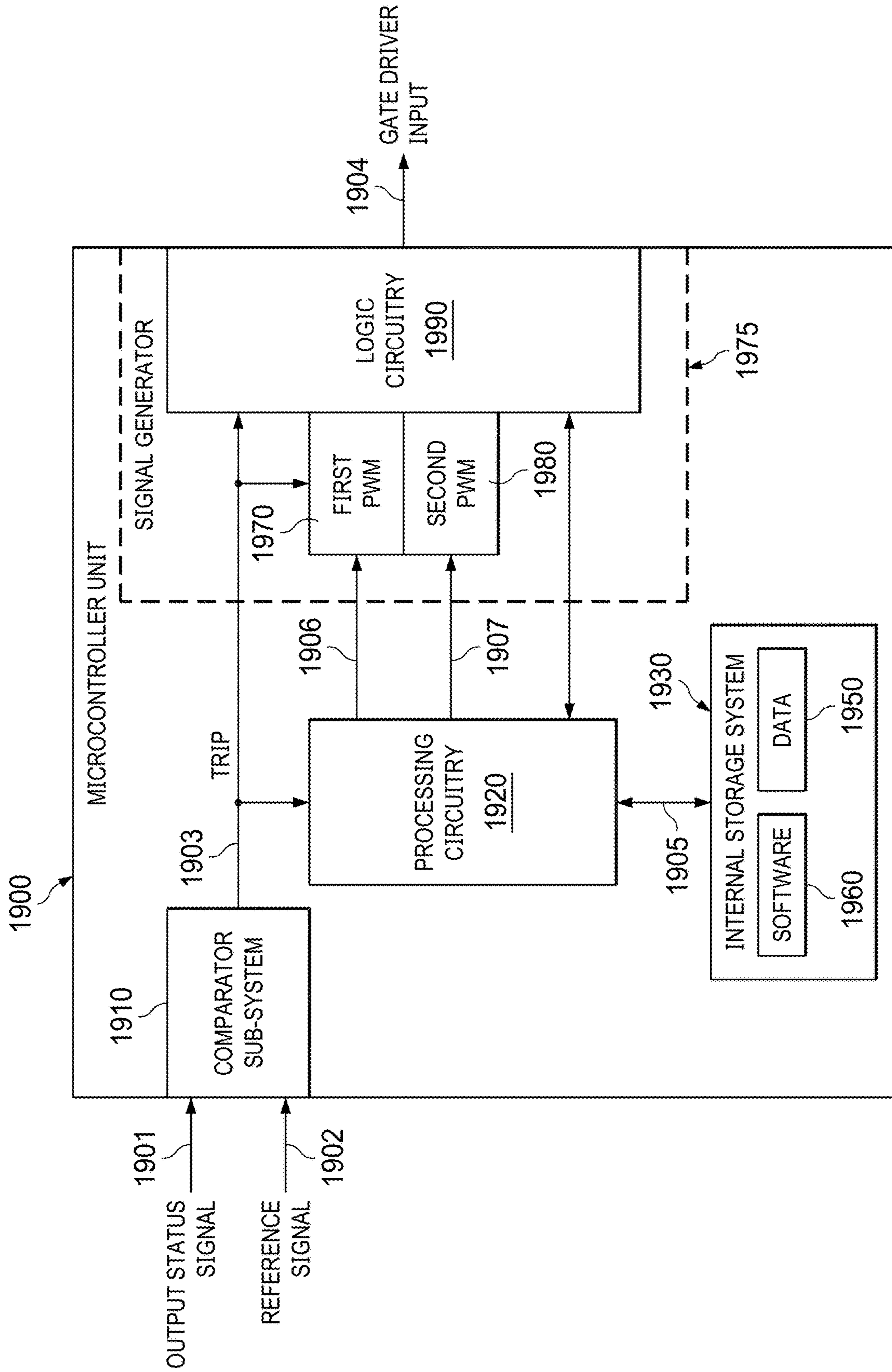


FIG. 19

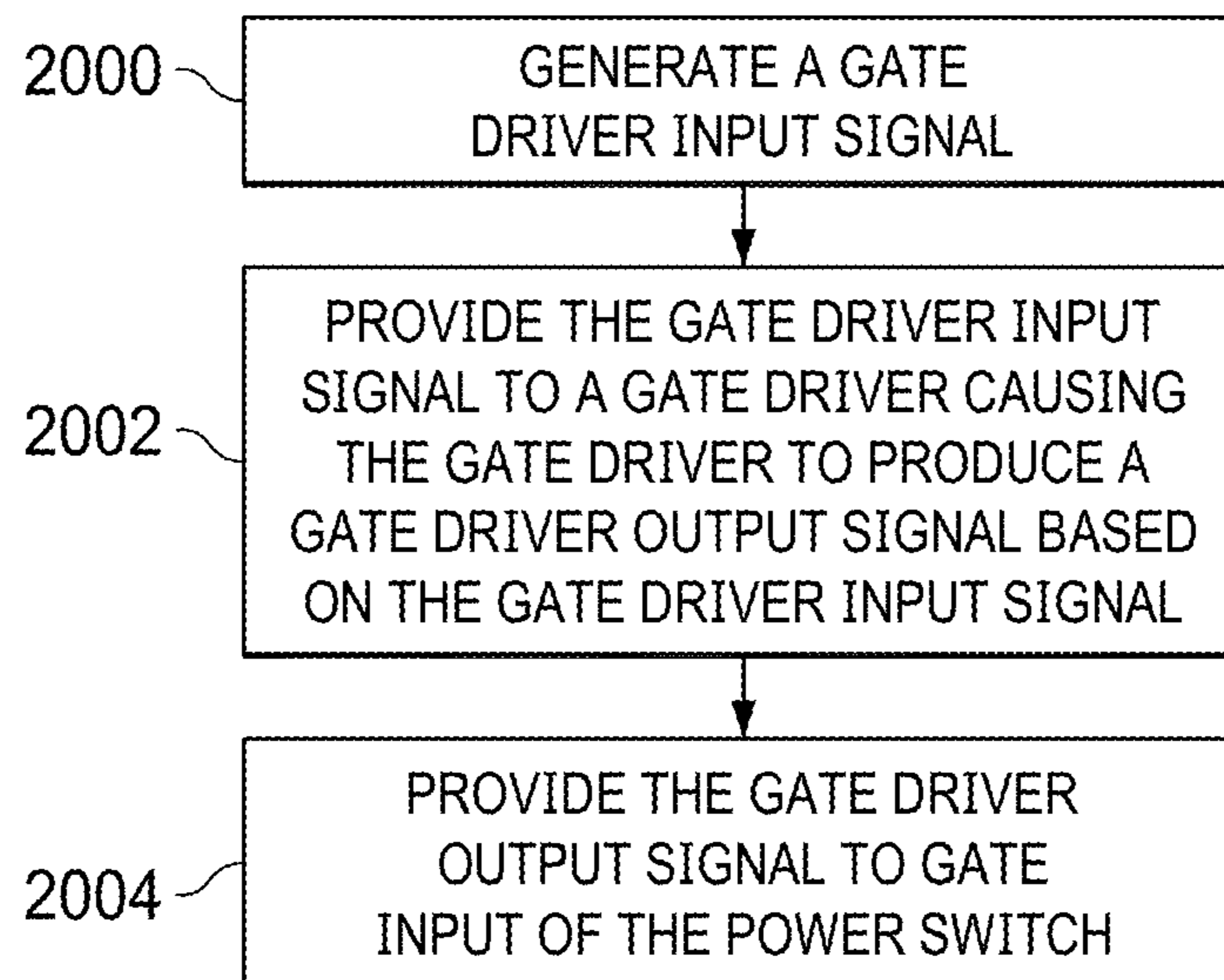


FIG. 20

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**CIRCUIT AND SYSTEM FOR THE
REDUCTION OF VOLTAGE OVERSHOOT IN
POWER SWITCHES**

CROSS-REFERENCE TO RELATED
APPLICATIONS

The present application is a continuation of U.S. patent application Ser. No. 17/820,424, filed Aug. 17, 2022, which is incorporated by reference herein in its entirety.

TECHNICAL BACKGROUND

Power modules are used in a large variety of applications including inverters, DC-DC converters, motor drives, power supplies, uninterruptible power supplies (UPS), and the like. These power modules are often constructed with power switches such as Insulated Gate Bipolar Transistors (IGBT) configured as a single half bridge or multiple half bridge inverters. IGBT power modules have parasitic inductances inherent in their constructions. These inductances are found in bond wires, package pins, metal patterns, soldering, and the like. When power switches are shut off very quickly, such as during an over current fault condition, these parasitic inductances create transient voltages within the power module. In some cases, these transient voltages are sufficient to physically damage the power switches.

OVERVIEW

In an implementation, an electronic circuit for controlling a power switch having a gate input includes a signal generator configured to generate a gate driver input signal. The gate driver input signal has a first voltage during a first period of time, a second voltage during a second period of time, and toggles between the first voltage and the second voltage during a third period of time.

The electronic circuit also includes a gate driver configured to receive the gate driver input signal and to provide a gate driver output signal to the gate input of the power switch based on the gate driver input signal. The signal generator is configured to cause the gate driver input signal to toggle during the third period of time such that the gate driver output signal has a third voltage during the second period of time, and an intermediate voltage that is less than the third voltage during the third period of time.

In another implementation, a microcontroller unit for controlling a power switch having a gate input includes a signal generator configured to generate a gate driver input signal. The gate driver input signal has a first voltage during a first period of time, a second voltage during a second period of time, and toggles between the first voltage and the second voltage during a third period of time.

The gate driver input signal, when provided to a gate driver causes the gate driver to provide a gate driver output signal to the gate input of the power switch based on the gate driver input signal. The signal generator is further configured to cause the gate driver input signal to toggle during the third period of time such that the gate driver output signal has a third voltage during the second period of time, and an intermediate voltage that is less than the third voltage during the third period of time.

In a further embodiment, a method for using a microcontroller unit to control a power switch having a gate input includes generating a gate driver input signal. The gate driver input signal has a first voltage during a first period of time, a second voltage during a second period of time, and

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toggles between the first voltage and the second voltage during a third period of time.

The method also includes providing the gate driver input signal to a gate driver causing the gate driver to produce a gate driver output signal based on the gate driver input signal, and providing the gate driver output signal to the gate input of the power switch.

The gate driver input signal toggles during the third period of time such that the gate driver output signal has a third voltage during the second period of time, and an intermediate voltage that is less than the third voltage during the third period of time.

BRIEF DESCRIPTION OF THE DRAWINGS

Many aspects of the disclosure can be better understood with reference to the following drawings. While several implementations are described in connection with these drawings, the disclosure is not limited to the implementations disclosed herein. On the contrary, the intent is to cover all alternatives, modifications, and equivalents.

FIG. 1 illustrates an example embodiment of an ideal half-bridge insulated gate bipolar transistor (IGBT) module.

FIG. 2 illustrates an example embodiment of a half-bridge insulated gate bipolar transistor (IGBT) module including parasitic inductances.

FIG. 3 illustrates an output of a simulation demonstrating transient voltages on a power module output due to parasitic inductances.

FIG. 4 illustrates a prior art example embodiment of a circuit designed to provide a two-level turn-off to a power module.

FIG. 5 illustrates an output of a simulation demonstrating reduced transient voltages on a power module output due to parasitic inductances when using a two-level turn-off.

FIG. 6A illustrates an example embodiment of a circuit designed to provide a two-level turn-off to a power module.

FIG. 6B illustrates example waveforms of signals within the circuit of FIG. 6A.

FIG. 7 illustrates an example embodiment of a circuit designed to provide a two-level turn-off to a power module.

FIG. 8 illustrates an example embodiment of a circuit designed to provide a two-level turn-off to a power module.

FIG. 9 illustrates outputs of a simulation of the circuit of FIG. 8 demonstrating a two-level turn-off using a microcontroller unit and a less complex gate driver.

FIG. 10 illustrates outputs of a simulation of the circuit of FIG. 8 demonstrating a maximum second pulse width modulator frequency.

FIG. 11 and FIG. 12 illustrate outputs of simulations of the circuit of FIG. 8 demonstrating the impact of an initial time delay in turning on the second pulse width modulator.

FIG. 13 and FIG. 14 illustrate outputs of simulations of the circuit of FIG. 8 demonstrating the impact of a change in the duty cycle of the second pulse width modulator.

FIG. 15 and FIG. 16 illustrate outputs of simulations of the circuit of FIG. 8 demonstrating the impact of a change in the pulse width of the second pulse width modulator.

FIG. 17 and FIG. 18 illustrate outputs of simulations of the circuit of FIG. 8 demonstrating the impact of a change in the resistor-capacitor (RC) components at the output of the second pulse width modulator.

FIG. 19 illustrates a block diagram of an example embodiment of a microcontroller unit configured to provide a two-level turn-off to a power module.

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FIG. 20 illustrates a flow chart of an example embodiment of a method for using a microcontroller unit to provide a two-level turn-off to a power module.

DETAILED DESCRIPTION

The following descriptions of various example embodiments and implementations of an electronic circuit for controlling a power switch illustrate systems and methods for reducing overshoot in a power switch when the switch is being shut down, such as during a fault. In these various examples a signal generator is configured to provide a gate driver input to a gate driver configured to drive the gate input of a power switch. In some examples, the signal generator includes first and second pulse width modulators (PWMs). A signal from the first PWM controls the gate driver during normal operation, and during a shut down the second PWM generates a higher frequency signal for combination with the signal from the first PWM such that the combined signal causes the gate driver output to provide an intermediate voltage to the gate input of the power switch while the second PWM is active.

By providing this intermediate voltage to the gate input of the power switch for a period of time during shutdown, overshoots due to parasitic inductances are reduced, preventing damage to the power switch. The various embodiments and implementations described herein provide a technical effect and technical advantage over other similar systems by providing the intermediate voltage using a less complex (inexpensive) gate driver rather than the complex (expensive) gate drivers able to produce the intermediate voltage on their own.

These complex gate drivers provide for setting the intermediate voltage with an external diode and capacitor. In some examples, complex gate drivers use a digital communication interface to set the intermediate voltage. In contrast, the present embodiments remove the need for these external components or interfaces and allow for the use of a less complex, less expensive gate driver. Since six gate drivers are used in many three-phase power converters, the cost and area savings from the elimination of the external diode and capacitor, and the replacement of a complex (expensive) gate driver with a less complex (less expensive) gate driver, is multiplied six-fold, providing a significant technical advantage over other solutions.

FIG. 1 illustrates an example embodiment of an ideal half-bridge insulated gate bipolar transistor (IGBT) module 100. In this embodiment, a half-bridge IGBT module 100 includes two IGBTs Q1 111 and Q2 112, along with two diodes D1 121 and D2 122. Power is supplied by power supply VCC 105 and a ground 106 is also provided. IGBT Q1 111 has a gate input IN1 101 and IGBT Q2 112 has a gate input IN2 102. The output 103 of the module is at the node connecting the emitter of Q1 111 with the collector of Q2 112.

FIG. 2 illustrates an example embodiment of a half-bridge insulated gate bipolar transistor (IGBT) module 200 including parasitic inductances. As discussed above, FIG. 1 is an idealized representation of a half-bridge IGBT module. In reality a number of parasitic inductances are actually present, both inherent in the devices, and due to package and board inductances. FIG. 2 illustrates the power module of FIG. 1 including these parasitic inductances.

In this embodiment, half-bridge IGBT module 200 includes two IGBTs Q1 211 and Q2 212, along with two diodes D1 221 and D2 222. Power is supplied by VCC 205 and a ground 206 is also provided. IGBT Q1 211 has a gate

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input IN1 201 and IGBT Q2 212 has a gate input IN2 202. The output 203 of the module is at a node connecting the emitter of Q1 211 with the collector of Q2 212 through parasitic inductors.

In this example, eight parasitic inductors are illustrated. Inductor LIU 231 represents inductance between VCC 205 and the cathode of diode D1 221. Inductor LC1 232 represents inductance between the cathode of diode D1 221 and the collector of IGBT Q1 211. Inductor LE1 233 represents inductance between the emitter of IGBT Q1 211 and the anode of diode D1 221. Inductor LIL represents inductance between the anode of diode D1 221 and the output 203. Inductor L2U represents inductance between the output 203 and the cathode of diode D2 222. Inductor LC2 236 represents inductance between the cathode of diode D2 222 and the collector of IGBT Q2 212. Inductor LE2 237 represents inductance between the emitter of IGBT Q2 212 and the anode of diode D2 222. Inductor L2L represents inductance between the anode of diode D2 222 and ground 206.

Note that this illustration is one possible representation of parasitic inductances found in a half-bridge IGBT module. Other embodiments may have some or all of these inductances, or other inductances not illustrated here depending on their design and construction.

Together these parasitic inductances cause transient voltages during switching of the IGBTs. The transient voltage may be calculated with the following equation:

$$\Delta V = -L_{\delta} \times \frac{di_{L_{\delta}}}{dt}$$

where ΔV is the transient voltage, L_{δ} is the parasitic inductance and

$$\frac{di_{L_{\delta}}}{dt}$$

is the rate of current change within the parasitic inductance.

During overcurrent fault conditions, di/dt can be very high and in some cases may exceed the voltage limit of V_{CE} (voltage across the collector to emitter) in the switch and subsequently damage the IGBT. An example of this overshoot is illustrated in FIG. 3.

FIG. 3 illustrates an output 300 of a simulation demonstrating transient voltages on a power module output due to parasitic inductances, along with an expanded view 320 of the transitions. In this example simulation, the input 302 to an IGBT (the voltage across the gate to emitter (V_{GE}) of the IGBT), the collector current (I_C) 304 of the IGBT, and the output voltage 306. In some examples, the output voltage is also the voltage across the collector to emitter (V_{CE}) of the IGBT. In this example V_{CC} is set to 400V DC and the IGBT is rated for 600V.

In this simulation, the input 302 is suddenly shut off, and when the voltage across the gate to emitter (V_{GE}) drops below the threshold voltage of the IGBT, the collector current (I_C) 304 drops, and the output 306 voltage sharply rises to an 870-volt peak 310 and a peak collector current (I_C) of about 712 amps 312 that falls to zero in approximately 1.75 usec. This 470-volt overshoot 310 above the 400V supply voltage (for a total of 870V) may be sufficient to damage IGBTs rated for 600V. In other examples, these values vary depending on the system design and use case.

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FIG. 4 illustrates a prior art example embodiment of a circuit 400 designed to provide a two-level turn-off to a power module. In order to prevent the damaging overshoot illustrated in FIG. 3, advanced gate drivers 420 may be used to provide a two-level turn-off to the gate of the IGBT. A two-level turn-off is when, while shutting off the gate, the gate driver applies an intermediate voltage to the gate for a quantity of time, before completely turning off the gate. This intermediate voltage is designed to be less than the normal high voltage applied to turn on the gate, and greater than the normal low voltage applied to turn off the gate. This is further illustrated in FIG. 6B and described below.

In this example, microcontroller unit 410 controls advanced gate driver 420 to provide a two-level turn-off to an IGBT. Microcontroller unit 410 provides input signal GD_IN 415 to advanced gate driver 420. The intermediate voltage of the two-level turn-off is set by diode D1 432 and capacitor C1 434 at input Intermediate Level Set 430. In this example diode D1 432 is a 10V diode, and capacitor C1 434 is a 47 pF capacitor. In this embodiment, a resistor R1 424 is connected between the output of advanced gate driver 420, GD_OUT 422, and the gate input (V_{GE}) 428 of the power switch. R1 424 is configured, in combination with capacitance C1 426 of the power switch, to add a resistor-capacitor (RC) time constant to GD_OUT 422 provided to the gate input of the power switch, V_{GE} 428.

FIG. 5 illustrates an output 500 of a simulation demonstrating reduced transient voltages on a power module output due to parasitic inductances when using a two-level turn-off. In this example simulation, the output of a gate driver GD_OUT 504 to an IGBT is illustrated along with the voltage across the gate to emitter (V_{GE}) 502 of the IGBT, the collector current (I_C) 506 of the IGBT, and the output voltage V_{CE} 508.

In this simulation, GD_OUT 504 includes an intermediate voltage for a period of time during a two-level turn-off, and when the voltage across the gate to emitter (V_{GE}) 502 drops below the threshold voltage of the IGBT, the collector current (I_C) 506 drops, and the output 308 sharply rises, however in contrast to the simulation illustrated in FIG. 3 the overshoot 510 is reduced to 583V. In many instances, this reduction is sufficient to protect the 600V rated IGBT from damage.

FIG. 6A illustrates an example embodiment of a circuit 600 designed to provide a two-level turn-off to a power module. In this example embodiment, by appropriately configuring a signal generator within a microcontroller unit 610, a gate driver 620 is sufficient to provide two-level turn-off inputs to a power module even if gate driver 620 does not have variable output settings. Since six gate drivers are used in many three-phase power converters, the cost and area savings from the elimination of diode D1 432 and capacitor C1 434 (of the circuit illustrated in FIG. 4), and the replacement of a complex (expensive) gate driver with a less complex (less expensive) gate driver, is multiplied six-fold.

In this example, microcontroller unit 610 is configured such that a gate driver input signal is generated from a signal generator within microcontroller unit 610 and provided to gate driver 620 causing the gate driver 620 to apply a two-level turn-off input to the gate of an IGBT in a power module and thus reduce the voltage overshoot during turn-off as illustrated in FIG. 5.

In this example, microcontroller unit 610 controls gate driver 620 to provide a two-level turn-off to an IGBT. Microcontroller unit 605 provides input signal GD_IN 615 to gate driver 620. The intermediate voltage of the two-level

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turn-off is set by appropriately configuring the signal generator. Gate driver 620 provides output GD_OUT 622 to the gate of the IGBT.

In this embodiment, a resistor R1 424 is connected between the output of gate driver 620, GD_OUT 622, and the gate input (V_{GE}) 628 of the power switch. R1 624 is configured, in combination with capacitance C1 626 of the power switch, to add a resistor-capacitor (RC) time constant to GD_OUT 622 provided to the gate input of the power switch, V_{GE} 628.

Further details of this circuit are illustrated in FIG. 7 and FIG. 8 and described in detail below.

FIG. 6B illustrates example waveforms 630 and 640 of signals GD_IN 615 and V_{GE} 628 within the circuit of FIG. 6A. In this example embodiment, a signal generator within microcontroller unit 610 is configured to generate a gate driver input signal, GD_IN 615. The gate driver input signal 615, illustrated by waveform 630, has a first voltage V1 632 during a first period of time (between time T_0 650 and T_1 651), a second voltage V2 634 during a second period of time (between time T_1 651 and T_2 652), and toggles between the first voltage V1 632 and the second voltage V2 634 during a configurable third period of time (between time T_2 652 and T_4 654).

In this embodiment, there is a configurable initial delay between time T_2 652 and T_3 653 before GD_IN 615 begins to toggle between V1 632 and V2 634. In various embodiments, the third period of time between time T_2 652 and T_4 654, the frequency of the pulses between time T_3 653 and T_4 654, the duty cycle of the pulses between time T_3 653 and T_4 654, and the number of pulses between time T_3 653 and T_4 654 are configurable in various combinations.

The voltage across the gate to emitter (V_{GE}) 628 of the IGBT is illustrated by waveform 640. During the first period of time (between times T_0 650 and T_1 651) V_{GE} 628 is at normal low gate driver output voltage V_{LOW} 646 and the IGBT is off. During the second period of time (between times T_1 651 and T_2 652) V_{GE} 628 is at normal high gate driver output voltage VHIGH 642 and the IGBT is conducting.

During the initial time delay in the third period of time (between times T_2 652 and T_3 653) while GD_IN 615 is at V1 632 and GD_OUT 622 is low, V_{GE} 628 falls from normal high gate driver output voltage VHIGH 642 to intermediate voltage V_{INT} 644 in a slope dependent on the RC time constant of resistor R1 624 and capacitance C1 626. At time T_3 653, GD_IN 615 begins to toggle, and V_{GE} 628 remains at V_{INT} 644 until the end of the third period of time at T_4 654. At the end of the third period of time GD_IN 615 drops to V1 632 and V_{GE} 628 drops to V_{LOW} 646 in a slope dependent on the RC time constant of resistor R1 624 and capacitance C1 626.

The gate driver output signal, GD_OUT 622, is not illustrated here, however it is similar to V_{GE} 628 without the RC delay effect. During the second period of time (between times T_1 651 and T_2 652) GD_OUT 622 is at a third voltage (the normal high gate driver output voltage). During the third period of time, while the gate driver input GD_IN 615 is toggling, the gate driver output GD_OUT 622 drops to an intermediate voltage that is less than the third voltage.

In some embodiments, the intermediate voltage is provided to the IGBT only when the power switch is being shut down, such as during a fault condition. FIG. 7 illustrates a system configured to detect a fault condition in the power switch and provide the intermediate voltage to the IGBT as the power switch is shut down due to the fault. In other

embodiments, a similar intermediate voltage at V_{GE} is provided during normal operation of the inverter

FIG. 7 illustrates an example embodiment of a circuit 700 designed to provide a two-level turn-off to a power module 750. FIG. 7 is a more detailed illustration of the circuit of FIG. 6. In some embodiments, microcontroller unit 710 is equivalent to microcontroller unit 610 of FIG. 6 and gate driver 740 is equivalent to gate driver 620 of FIG. 6. In this example, microcontroller unit 710 is configured to provide a gate driver input signal GD_IN 703 to gate driver 740 such that gate driver 740 provides a gate driver output signal V_{GE} 704 to the input gate of IGBT Q2 754 within half-bridge inverter 750 providing an intermediate voltage level to V_{GE} 704 during turn-off. In this illustration, the RC circuit of resistor R1 624 and capacitance C1 626 from FIG. 6A is not shown. In this embodiment, microcontroller unit 710 includes processing circuitry 720, signal generator 730, and comparator sub-system 770. Processing circuitry 720 is configured to control signal generator 730 and is coupled with various circuits within signal generator 730.

In this example, microcontroller unit 710 and gate driver 740 are used to drive one IGBT (Q2 754) within IGBT half-bridge inverter 750. IGBT half-bridge inverter 750 includes IGBTs Q1 752 and 754, and diodes D1 753 and D2 755. Power is supplied at V_{cc} 751, and a ground 756 is provided. The output 757 of inverter 750 is monitored for fault conditions by current sensor 758 that provides a current signal 705 to signal conditioning circuitry 760 that in turn provides an output status signal 706 to comparator sub-system 770 within microcontroller unit 710. In some embodiments signal conditioning circuitry 760 is also included within microcontroller unit 710. Comparator sub-system 770 includes comparator 772 and filter and digital logic 774. In this embodiment, comparator 772 receives output status signal 706 from signal conditioning circuitry 760 and compares it to reference signal 707. Comparator 772 generates an output whenever output status signal 706 exceeds reference signal 707. The output of the comparator is filtered and the logic level may be modified by the filter and digital logic 774. Filter and digital logic 774 generate fault signal TRIP 709 upon detection of an over current fault within IGBT half-bridge inverter 750 based on the signal from current sensor 758 or other signals not shown in FIG. 7.

In this example embodiment, signal generator includes first PWM 732, second PWM 734 and logic circuitry 736. In this example, first PWM 732 produces a first signal 701 having a first frequency that is used to drive the input GD_IN 703 to gate driver 740 during normal operation. Second PWM 734 produces a second signal 702 having a second frequency higher than the first frequency that is used to modify the first signal 701 from first PWM 732 using logic circuitry 736 during turn-off in order to produce a two-level turn-off. Second PWM 734 is highly configurable such that the frequency, duty cycle, number of pulses, delay, and the like of its output pulses may be configured in order to best control the two-level turn-off in order to minimize overshoot. In some example embodiments, values for the configurable settings of second PWM 734 are stored in an internal storage system within microcontroller 710.

When an over current fault is detected from output status signal 706, comparator sub-system 770 provides TRIP signal 709 to first PWM 732, second PWM 734, and logic circuitry 736 such that for a period of time during turn-off of inverter 750, second PWM 734 is activated and is used to modify the signal from first PWM 732 in order to produce a gate driver input signal GD_IN 703 that is provided to gate

driver 740. After the period of time ends, and the half-bridge inverter 750 is shut down, first PWM 732 and second PWM 734 are shut down.

In some example embodiments, the output of the first PWM 732 remains high while second PWM 734 is active and logic circuitry 736 provides an AND function to the two PWM outputs. In other example embodiments, the output of the first PWM 732 is low while second PWM 734 is active and logic circuitry provides an OR function to the two PWM outputs. In still other example embodiments, the second PWM 734 is active during each cycle of the first PWM 732 regardless of whether or not a fault is detected. A wide variety of embodiments of signal generator 730 may be implemented to provide GD_IN 703 similar to the waveform 630 illustrated in FIG. 6B, all within the scope of the present invention.

The gate of Q1 752 is driven by a second signal generator within microcontroller unit 710 and an additional gate driver similar to gate driver 740. As discussed above, in three-phase power converters microcontroller unit 710 includes six instantiations of signal generator 730 configured to drive six gate drivers similar to gate driver 740. Each of the six gate drivers drive the gate of one IGBT within the three-phase power converter. Each of the six signal generators and gate drivers are configured to operate as described above.

FIG. 8 illustrates an example embodiment of a circuit 800 designed to provide a two-level turn-off to a power module. FIG. 8 is a more detailed illustration of the circuit of FIGS. 6 and 7. In some embodiments, microcontroller equivalent circuit 810 is equivalent to microcontroller unit 710 of FIG. 7 and microcontroller unit 610 of FIG. 6, and gate driver 838 is equivalent to gate driver 740 of FIG. 7 and gate driver 620 of FIG. 6. In this example, the logical path of signals from first PWM 824 and second PWM 816 through gate driver 838 to the gate input of a power switch V_{GE} 846 is illustrated. In this example, an equivalent circuit 810 for a portion of a microcontroller unit is illustrated to show how the first signal from first PWM 824 is modified by the second signal from second PWM 816. Example logic circuitry 811 is illustrated to show the combination of these signals. However, this is one example of how these signals may be combined, and other embodiments use other circuits and methods to combine or generate a combined signal all within the scope of the present invention.

In this example embodiment comparator subsystem COMP 812 generates TRIP 814, first PWM 824 generates a first signal 826 having a first frequency, and second PWM 816 generates a second signal 818 having a second frequency higher than the first frequency. TRIP 814 and the second signal 818 are inputs to AND gate 820, while TRIP 814 is inverted by inverter 822 and, along with the first signal 826, is an input to AND gate 828. The outputs of AND gates 820 and 828 are inputs to OR gate 830 which produces output 832 from the MCU equivalent circuit 810.

The output 832 from MCU equivalent circuit 810 is provided to gate driver 838 as gate driver input 836 after passing through resistor R2 834. Gate driver 838 produces gate driver output 840. In some embodiments, a resistor R1 842 is connected between the output of gate driver 838 and the gate input 846 of the power switch, configured, in combination with a capacitance C1 844 of the power switch, to add a resistor-capacitor (RC) time constant to the output of the gate driver 838 provided to the gate input of the power switch, V_{GE} . The effect of this additional RC time constant is illustrated in FIG. 17 and FIG. 18 and discussed below.

FIGS. 9-18 illustrate outputs of various simulations of the control circuit illustrated in FIG. 7 and FIG. 8. Each of these

simulation outputs include waveforms for the gate driver input at node **836** of FIG. **8**, the gate driver output at node **840** of FIG. **8** and the gate input of the power switch, V_{GE} at node **846** of FIG. **8**. The following simulation outputs illustrate various effects of different configuration of second PWM **816** including different frequencies, duty cycles, number of pulses, and initial delay.

FIG. **9** illustrates outputs **900** and **910** of a simulation of the circuit of FIG. **8** demonstrating a two-level turn-off using a microcontroller unit and a less complex gate driver. In this example, simulation gate driver input **912** has a pulse width of 125 ns, a period of 140 ns and an initial delay of 150 ns. Here, second PWM **816** is operational for a total of 3 us during turn-off. Gate driver output **904** has a pulse width of 90 ns, and V_{GE} **902** has an intermediate voltage of about 9.6V.

FIG. **10** illustrates outputs **1000** and **1010** of a simulation of the circuit of FIG. **8** demonstrating a maximum second pulse width modulator frequency. In this example simulation gate driver input **1012** has a pulse width of 50 ns, a period of 65 ns and an initial delay of 50 ns. In this example, the frequency of second PWM **816** is too high for gate driver **838**, and it stops functioning as seen by gate driver output **1002** and V_{GE} **1004**.

FIG. **11** and FIG. **12** illustrate outputs **1100**, **1110**, **1200**, and **1210** of simulations of the circuit of FIG. **8** demonstrating the impact of an initial time delay in turning on the second pulse width modulator. In the simulation of FIG. **11**, gate driver input **1112** has a pulse width of 125 ns, a period of 140 ns, and an initial time delay of 0 ns. Gate driver output **1102** has a very small initial time delay **1114** which does not give the RC circuit of resistor R1 **842** and capacitor C1 **844** time to lower the voltage of V_{GE} **846** before the output of gate driver **838** begins cycling. As a result, V_{GE} **1104** slowly drops to the desired intermediate value.

In contrast, in the simulation of FIG. **12**, gate driver input **1212** has a pulse width of 125 ns, a period of 140 ns, and an initial time delay of 150 ns. In response, gate driver output **1202** has a longer initial time delay **1214** which allows the RC circuit of resistor R1 **842** and capacitor C1 **844** time to lower the voltage of V_{GE} **846** before the output of gate driver **838** begins cycling. As a result, V_{GE} **1204** drops to the desired intermediate value during the initial time delay **1214** and remains stable for the rest of the two-level turn-off.

FIG. **13** and FIG. **14** illustrate outputs **1300**, **1310**, **1400**, and **1410** of simulations of the circuit of FIG. **8** demonstrating the impact of a change in the duty cycle of the second pulse width modulator. In the simulation of FIG. **13**, gate driver input **1312** has a pulse width of 125 ns, a period of 175 ns, and an initial time delay of 150 ns. Gate driver output **1302** and V_{GE} **1304** show normal operation as a two-level turn-off.

In the simulation of FIG. **14**, gate driver input **1412** has a pulse width of 125 ns, a period of 200 ns, and an initial time delay of 150 ns. Gate driver output **1402** and V_{GE} **1404** show normal operation as a two-level turn-off, substantially the same as illustrated in FIG. **13**, demonstrating that duty cycle has little effect on V_{GE} **1404**.

FIG. **15** and FIG. **16** illustrate outputs **1500**, **1510**, **1600**, and **1610** of simulations of the circuit of FIG. **8** demonstrating the impact of a change in the pulse width of the second pulse width modulator. In the simulation of FIG. **15**, gate driver input **1512** has a pulse width of 250 ns, a period of 265 ns, and an initial time delay of 100 ns. Gate driver output **1502** reflects the pulse width of gate driver input **1512** and V_{GE} **1504** stabilizes at about 11.5V with 1.4V of ripple.

In the simulation of FIG. **16**, gate driver input **1612** has a pulse width of 250 ns, a period of 280 ns, and an initial time delay of 150 ns. Gate driver output **1602** reflects the pulse width of gate driver input **1612** and V_{GE} **1604** stabilizes at about 10.7V with 1.8V of ripple, demonstrating the effect of pulse width on the voltage and ripple of V_{GE} **1604**.

FIG. **17** and FIG. **18** illustrate outputs **1700**, **1710**, **1800**, and **1810** of simulations of the circuit of FIG. **8** demonstrating the impact of a change in the RC components at the output of the gate driver. In the simulation of FIG. **17**, gate driver input **1712** has a pulse width of 250 ns, a period of 265 ns, and an initial time delay of 50 ns. Resistor R1 **842** has a value of 33 ohms and capacitor C1 **844** has a value of 4.7 nF. Gate driver output **1702** has a pulse width of 215 ns and V_{GE} **1704** stabilizes at about 12V with 3.4V of ripple.

In the simulation of FIG. **18**, gate driver input **1812** has a pulse width of 100 ns, a period of 115 ns, and an initial time delay of 50 ns. Resistor R1 **842** has a value of 15 ohms and capacitor C1 **844** has a value of 2.2 nF. Gate driver output **1802** has pulse width of 66 ns and V_{GE} **1804** stabilizes at about 8.7V with 2V of ripple, demonstrating the effect of the resistor-capacitor (RC) time constant and second PWM frequency on the voltage and ripple of V_{GE} **1804**. Lower RC time constants result in higher ripple, while higher frequencies result in higher distortion.

FIG. **19** illustrates a block diagram of an example embodiment of a microcontroller unit **1900** configured to provide a two-level turn-off to a power module. FIG. **19** is a more detailed illustration of the microcontroller unit of FIGS. **6-8**. In some embodiments, microcontroller unit **1900** is equivalent to microcontroller equivalent circuit **810**, microcontroller unit **710** of FIG. **7**, and microcontroller unit **610** of FIG. **6**. As discussed above, microcontroller unit **1900** may take on any of a wide variety of configurations. Here, a simplified example configuration is provided for a microcontroller unit **610** as illustrated in FIG. **6** and described above.

In this example embodiment, microcontroller unit **1900** comprises comparator sub-system **1910**, processing circuitry **1920**, first PWM module **1970**, second PWM module **1980**, logic circuitry **1990**, and internal storage system **1930**. In this embodiment, first PWM module **1970**, second PWM module **1980**, and logic circuitry **1990** together comprise signal generator **1975**. Comparator sub-system **1910** comprises circuitry configured to receive an output status signal **1901** from an output conditioner such as signal conditioning circuitry **760** from FIG. **7** described above. First PWM module **1970** is a pulse width modulator configured to provide a first signal having a first frequency, such as first PWM **732** from FIG. **7** described above. Second PWM module **1980** is a PWM configured to provide a second signal having a second frequency higher than the first frequency, such as second PWM **734** from FIG. **7** described above. Comparator sub-system **1910** is also configured to provide a TRIP signal **1903** to first PWM **1970**, second PWM **1980**, and logic circuitry **1990**. Logic circuitry **1990** is configured to process the first signal and the second signal to produce a gate driver input signal **1904** based on the first and second signals, similar to logic circuitry **811** from FIG. **8** described above.

Processing circuitry **1920** comprises electronic circuitry configured to direct microcontroller unit **1900** to provide a two-level turn-off as described above. Processing circuitry **1920** may comprise microprocessors and other circuitry that retrieves and executes software **1960**. Examples of processing circuitry **1920** include general purpose central processing units, application specific processors, and logic devices,

as well as any other type of processing device, combinations, or variations thereof. Processing circuitry **1920** can be implemented within a single processing device but can also be distributed across multiple processing devices or sub-

systems that cooperate in executing program instructions. Internal storage system **1930** can comprise any non-transitory computer readable storage media capable of storing software **1960** that is executable by processing circuitry **1920**. Internal storage system **1930** can also include various data structures **1950** which comprise one or more registers, databases, tables, lists, or other data structures. Storage system **1930** can include volatile and nonvolatile, removable and non-removable media implemented in any method or technology for storage of information, such as computer readable instructions, data structures, program modules, or other data. In this example embodiment, internal storage system **1930** includes flash memory within microcontroller unit **1900** which also stores configuration information for second PWM **1980**.

Storage system **1930** can be implemented as a single storage device but can also be implemented across multiple storage devices or sub-systems co-located or distributed relative to each other. Storage system **1930** can comprise additional elements, such as a controller, capable of communicating with processing circuitry **1920**. Examples of storage media include random access memory, read only memory, magnetic disks, optical disks, flash memory, virtual memory and non-virtual memory, magnetic cassettes, magnetic tape, magnetic disk storage or other magnetic storage devices, or any other medium which can be used to store the desired information and that can be accessed by an instruction execution system, as well as any combination or variation thereof.

Software **1960** can be implemented in program instructions and among other functions can, when executed by microcontroller unit **1900** in general or processing circuitry **1920** in particular, direct microcontroller unit **1900**, or processing circuitry **1920**, to operate as described herein to control a power switch. Software **1960** can include additional processes, programs, or components, such as operating system software, database software, or application software. Software **1960** can also comprise firmware or some other form of machine-readable processing instructions executable by elements of processing circuitry **1920**.

In at least one example implementation, the program instructions include various modules configured to direct processing circuitry **1920** to control first PWM module **1970**, second PWM module **1980**, and logic circuitry **1990** to produce two-level turn-off for a power switch as described above.

In general, software **1960** can, when loaded into processing circuitry **1920** and executed, transform processing circuitry **1920** overall from a general-purpose computing system into a special-purpose computing system customized to operate as described herein for a microcontroller unit **1900** configured to control a power switch, among other operations. Encoding software **1960** on internal storage system **1930** can transform the physical structure of internal storage system **1930**. The specific transformation of the physical structure can depend on various factors in different implementations of this description. Examples of such factors can include, but are not limited to the technology used to implement the storage media of internal storage system **1930** and whether the computer-storage media are characterized as primary or secondary storage.

For example, if the computer-storage media are implemented as semiconductor-based memory, software **1960** can

transform the physical state of the semiconductor memory when the program is encoded therein. For example, software **1960** can transform the state of transistors, capacitors, or other discrete circuit elements constituting the semiconductor memory. A similar transformation can occur with respect to magnetic or optical media. Other transformations of physical media are possible without departing from the scope of the present description, with the foregoing examples provided only to facilitate this discussion.

FIG. **20** illustrates a flow chart of an example embodiment of a method for using a microcontroller unit **710** to provide a two-level turn-off to a power module.

In this example method, microcontroller unit **710** produces a gate driver input signal GD_IN **703** from a signal generator **730**, (operation **2000**). The gate driver input signal GD_IN **703** has a first voltage during a first period of time, a second voltage during a second period of time, and toggles between the first voltage and the second voltage during a configurable third period of time.

Microcontroller unit **710** provides the gate driver input signal GD_IN **703** to a gate driver **740** causing the gate driver **740** to produce a gate driver output signal V_{GE} **704** based on the gate driver input signal GD_IN **703**, (operation **2002**).

Gate driver **740** provides the gate driver output signal V_{GE} **704** to the gate input of the power switch **750**, (operation **2004**). The gate driver input signal GD_IN **703** toggles during the third period of time such that the gate driver output signal V_{GE} **704** has a third voltage during the second period of time, and an intermediate voltage V_{INT} **644** less than the third voltage during the third period of time.

The included descriptions and figures depict specific embodiments to teach those skilled in the art how to make and use the best mode. For the purpose of teaching inventive principles, some conventional aspects have been simplified or omitted. Those skilled in the art will appreciate variations from these embodiments that fall within the scope of the invention. Those skilled in the art will also appreciate that the features described above may be combined in various ways to form multiple embodiments. As a result, the invention is not limited to the specific embodiments described above, but only by the claims and their equivalents.

What is claimed is:

1. A circuit device comprising:
a signal generator that includes:

a first pulse-width modulation circuit that includes an input and an output configured to provide a first signal;

a second pulse-width modulation circuit that includes an input and an output configured to provide a second signal; and

circuitry that includes:

a first input coupled to the output of the first pulse-width modulation circuit;

a second input coupled to the output of the second pulse-width modulation circuit; and

an output configured to provide a third signal based on at least one of the first signal and the second signal; and

processing circuitry coupled to the input of the first pulse-width modulation circuit and the input of the second pulse-width modulation circuit, wherein:

the processing circuitry includes an input configured to receive a current signal; and

the processing circuitry is configured to, based on the current signal, select between:

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causing the signal generator to operate in a first mode in which the third signal is determined by the first signal; and

causing the signal generator to operate in a second mode in which the third signal is determined by the second signal.

2. The circuit device of claim 1, wherein the second mode is such that a gate-to-emitter voltage of a power converter coupled to the output of the circuitry decreases to substantially zero volts during the second mode.

3. The circuit device of claim 1, wherein: in the first mode, a gate driver coupled to the output of the circuitry provides a first voltage; and in the second mode, the gate driver provides a second voltage that is less than the first voltage.

4. The circuit device of claim 1 further comprising a gate driver that includes: an input coupled to the output of the circuitry; and an output.

5. The circuit device of claim 4 further comprising a power converter circuit that includes a transistor that includes a gate coupled to the output of the gate driver.

6. The circuit device of claim 5, wherein: the power converter circuit further includes an output; and the transistor further includes: a collector coupled to the output of the power converter circuit; and an emitter coupled to ground.

7. The circuit device of claim 6, wherein: the transistor is a first transistor; and the power converter circuit further includes a second transistor that includes: a collector coupled to a voltage supply node; and an emitter coupled to the output of the power converter circuit.

8. The circuit device of claim 1, wherein: the circuitry is a first set of circuitry; and the circuit device further comprises:

a comparator that includes: a first input configured to receive a current measurement; a second input configured to receive a reference measurement; and an output; and

a second set of circuitry that includes: an input coupled to the output of the comparator; and an output coupled to the input of the processing circuitry and configured to provide the current signal.

9. The circuit device of claim 1, wherein the current signal is associated with an over-current condition.

10. A circuit device comprising:

a signal generator that includes:

a first pulse-width modulation circuit that includes an input and an output configured to provide a first signal;

a second pulse-width modulation circuit that includes an input and an output configured to provide a second signal; and

circuitry that includes:

a first input coupled to the output of the first pulse-width modulation circuit;

a second input coupled to the output of the second pulse-width modulation circuit; and

an output configured to provide a third signal based on at least one of the first signal and the second signal; and

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processing circuitry coupled to the input of the first pulse-width modulation circuit and the input of the second pulse-width modulation circuit, wherein the processing circuitry is configured to:

cause the signal generator to operate in a first mode in which the third signal is determined by the first signal and the third signal has a first frequency; and

cause the signal generator to operate in a second mode in which the third signal is determined by the second signal and the third signal has a second frequency that is greater than the first frequency, wherein the second mode is associated with a power converter coupled to the output of the circuitry being shut off.

11. A circuit device comprising:

a signal generator that includes:

a first pulse-width modulation circuit that includes an input and an output configured to provide a first signal;

a second pulse-width modulation circuit that includes an input and an output configured to provide a second signal; and

a first set of circuitry that includes:

a first input coupled to the output of the first pulse-width modulation circuit;

a second input coupled to the output of the second pulse-width modulation circuit; and

an output configured to provide a third signal based on at least one of the first signal and the second signal;

processing circuitry coupled to the input of the first pulse-width modulation circuit and the input of the second pulse-width modulation circuit, wherein the processing circuitry is configured to:

cause the signal generator to operate in a first mode in which the third signal is determined by the first signal and the third signal has a first frequency; and

cause the signal generator to operate in a second mode in which the third signal is determined by the second signal and the third signal has a second frequency that is greater than the first frequency;

a comparator; and

a second set of circuitry coupled between the comparator and the processing circuitry and configured to cause the processing circuitry to transition the signal generator to the second mode.

12. A system comprising:

a first pulse-width modulation circuit that includes an output configured to provide a first signal;

a second pulse-width modulation circuit that includes an output configured to provide a second signal;

a first set of circuitry that includes:

a first input coupled to the output of the first pulse-width modulation circuit;

a second input coupled to the output of the second pulse-width modulation circuit; and

an output configured to provide a third signal based on at least one of the first signal and the second signal, wherein the system is configured to:

operate in a first mode in which the third signal is determined by the first signal; and

operate in a second mode in which the third signal is determined by the second signal;

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a gate driver that includes:
 an input coupled to the output of the first set of
 circuitry; and
 an output configured to provide a gate voltage;
 a comparator; and
 a second set of circuitry coupled to the comparator and
 configured to cause the system to transition to the
 second mode.

13. The system of claim **12**, wherein the second mode is
 associated with a power converter coupled to the output of
 the gate driver being shut off.

14. The system of claim **12**, wherein the second mode is
 such that a gate-to-emitter voltage of a power converter
 coupled to the output of the gate driver decreases to sub-
 stantially zero volts during the second mode.

15. The system of claim **12**, wherein:
 in the first mode, the gate voltage has a first voltage value;
 and
 in the second mode, the gate voltage has a second voltage
 value that is less than the first voltage value.

16. The system of claim **12** further comprising a power
 converter circuit that includes a transistor that includes a
 gate coupled to the output of the gate driver.

17. The system of claim **16**, wherein:
 the power converter circuit further includes an output; and
 the transistor further includes:
 a collector coupled to the output of the power converter
 circuit; and
 an emitter coupled to ground.

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18. The system of claim **17**, wherein:
 the transistor is a first transistor; and
 the power converter circuit further includes a second
 transistor that includes:
 a collector coupled to a voltage supply node; and
 an emitter coupled to the output of the power converter
 circuit.

19. The system of claim **12**, wherein the second set of
 circuitry is configured to cause the system to transition to the
 second mode based on an over-current condition.

20. A method comprising:
 providing a first pulse-width modulated signal that has a
 first frequency;
 providing a second pulse-width modulated signal that has
 a second frequency that is greater than the first fre-
 quency;
 receiving a current signal; and
 based on the current signal, selecting between:
 in a first mode of operation, providing a third pulse-
 width modulated signal based on the first pulse-
 width modulated signal; and
 in a second mode of operation, providing the third
 pulse-width modulated signal based on the second
 pulse-width modulated signal.

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